

AM64x/AM243x EVM BOARD

PROC101C

TABLE OF CONTENTS

PAGE	CONTENTS
01	TABLE OF CONTENTS
02	REVISION HISTORY
03	BLOCK DIAGRAM AM64x EVM BOARD
04	BLOCK DIAGRAM - XDS110
05	POWER FLOW DIAGRAM
06	POWER SEQUENCE
07	GPIO MAPPING TABLE
08	I2C TREE
09	SOC POWER
10	SOC POWER CAPS
11	SOC VSS
12	DDR INTERFACE
13	eMMC FLASH AND SDCARD INTERFACE
14	OSPI FLASH
15	EEPROM, PRESENCE DETECTION & TEMP SENSOR
16	CPSW RGMII_1 ETHERNET PHY
17	ICSSG RGMII_2 ETHERNET PHY
18	ICSSG RGMII_1 ETHERNET PHY
19	TEST AUTOMATION
20	BOOT MODE BUFFER & SWITCHES
21	CURRENT MONITORING DEVICES
22	XDS110 DEBUGGER
23	JTAG BUFFER
24	MIPI 60 PIN CONNECTOR
25	USB 2.0 INTERFACE
26	FT4232 UART TO USB BRIDGE
27	HSE BOARD CONNECTOR
28	GPMC & FSI CONNECTOR
29	CAN & DISPLAY INTERFACE
30	PCIe INTERFACE
31	ETHERNET PHY & PCIe CLOCK GENERATOR
32	ETHERNET LEDs
33	IO EXPANDER & TEST HEADER
34	MCU GENERAL&SAFETY CONNECTOR

PAGE	CONTENTS
35	DEBOUNCE CIRCUIT & VOLTAGE SUPERVISOR
36	MAIN INPUT 12V DC
37	DUAL & PRE_REG POWER SUPPLY
38	SoC POWER SUPPLY
39	PERIPHERAL POWER SUPPLY
40	HARDWARE SCHEMATICS

REV	C
VER	1.1

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Title TABLE OF CONTENTS

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 1 of 40

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	11th MARCH 2022	Drafted from "PROC101B_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	11th MARCH 2022	Removed Voltage Monitor circuit & added RC Delay Circuit for power down sequence requirement Fixed Power down sequence issue seen on AM243x REV B	Mistral Design Team	AJIT MB	AJIT MB
0.3	11th MARCH 2022	Updated schematics to support PG2 Silicon	Mistral Design Team	AJIT MB	AJIT MB
1.0	30th MARCH 2022	Baselined and Released	Mistral Design Team	AJIT MB	AJIT MB
1.1	5th AUG 2022	Updated SoC Part Number and OPN Details Updated SoC Symbol for Reserved pins	Mistral Design Team	AJIT MB	AJIT MB

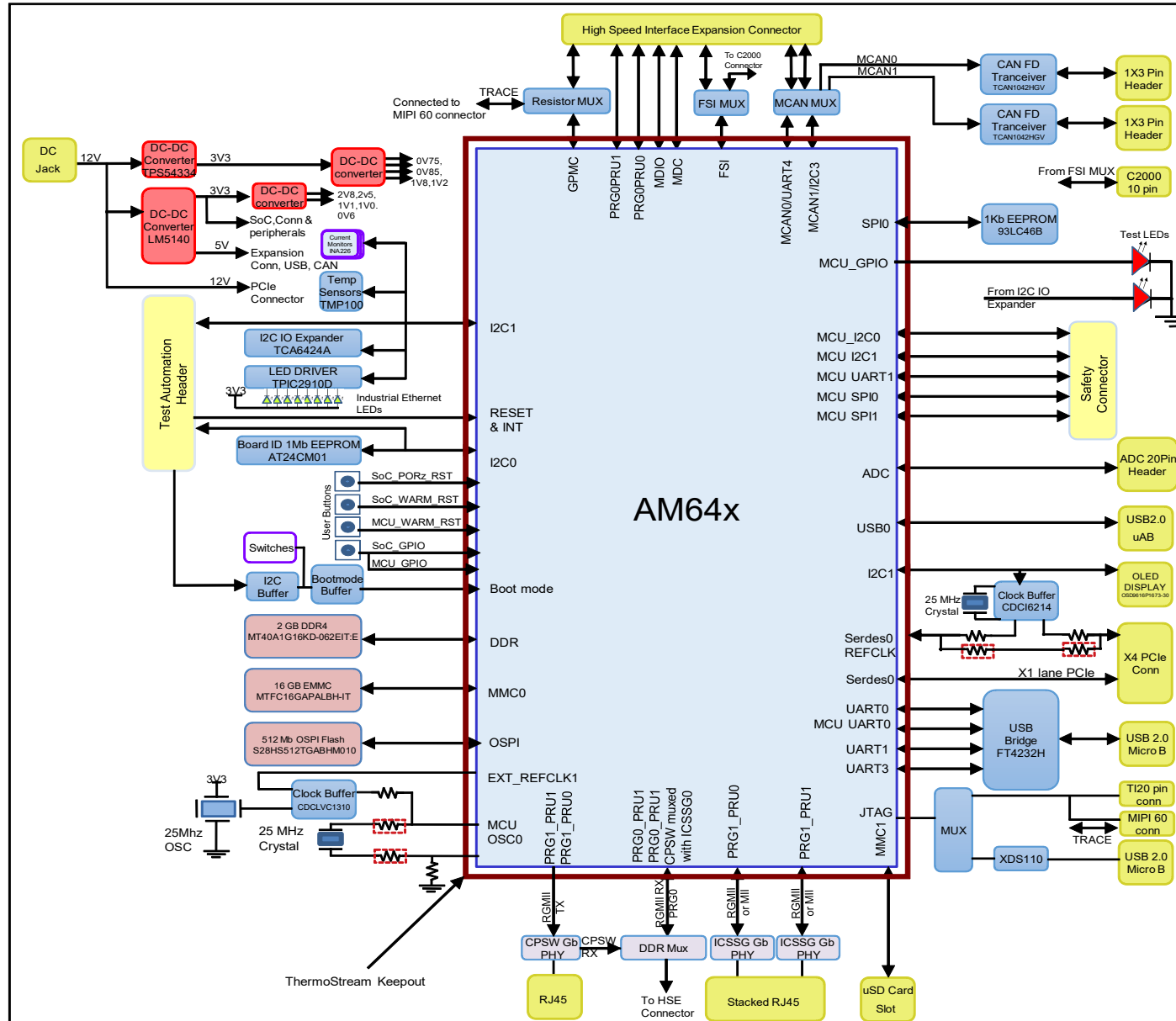
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Title REVISION HISTORY

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 2 of 40

BLOCK DIAGRAM_AM64x_EVM



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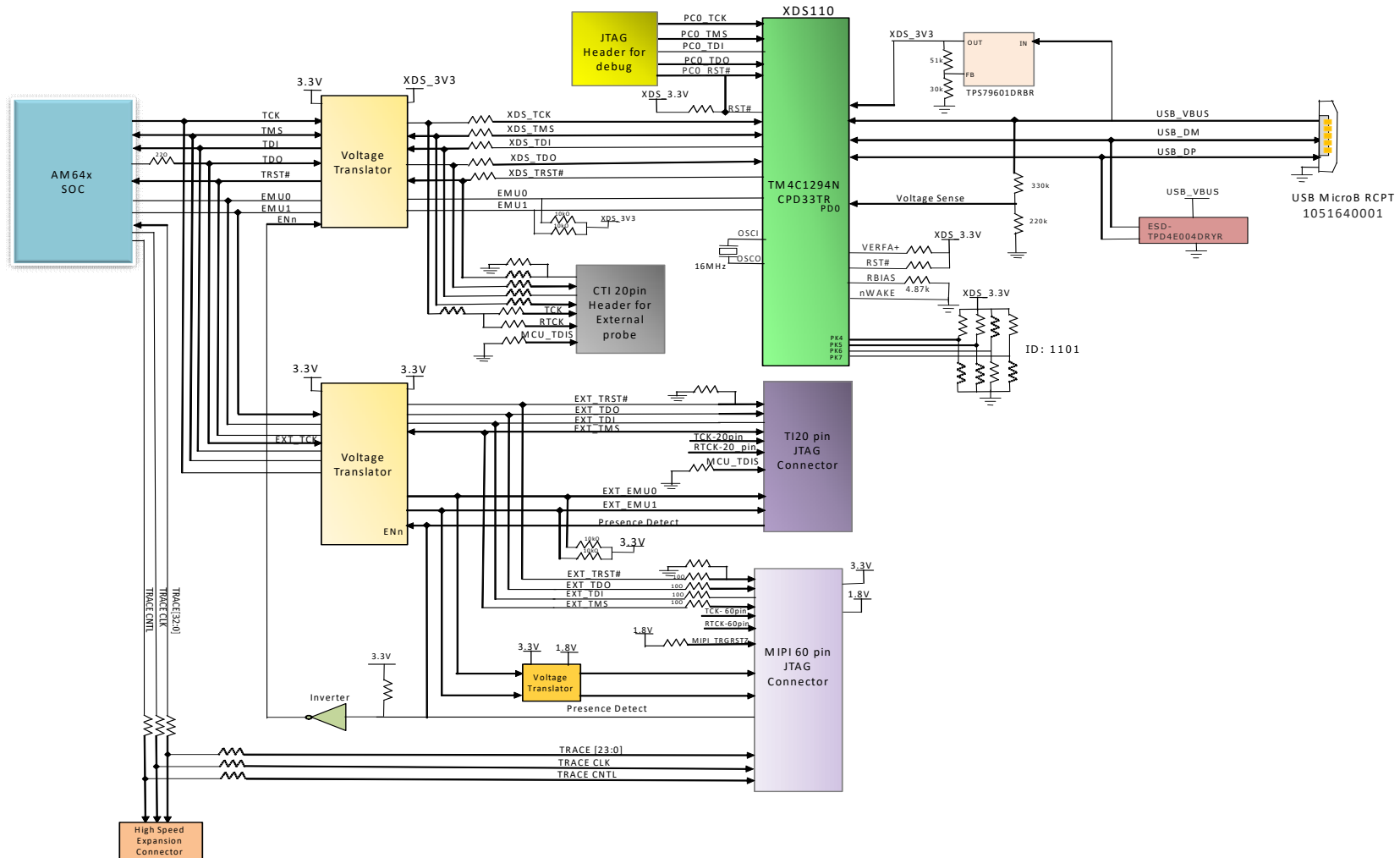
Title	BLOCK DIAGRAM_CP BOARD
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Size	Variant Name = PROC101C(005) TMD5243EVM
C	

Date:	Thursday, August 18, 2022	Sheet	3	of	40
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Rev
E2

BLOCK DIAGRAM_XDS110



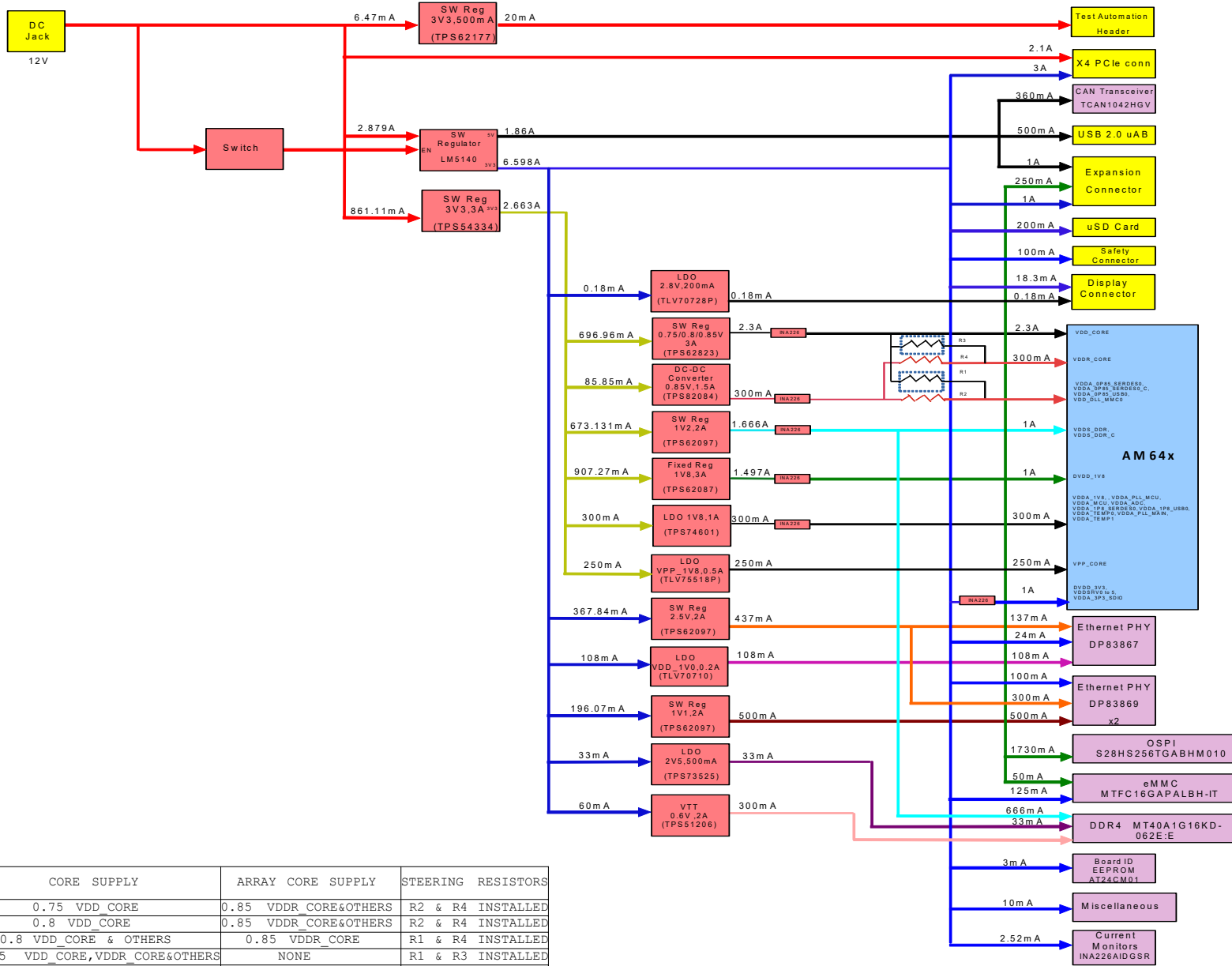
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Title BLOCK DIAGRAM_XDS110

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 4 of 40

POWER FLOW DIAGRAM



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Title POWER FLOW DIAGRAM

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 5 of 40

DC Jack

12V

Control From Test Automation Header

Switch

Voltage Monitor TPS3711

5V from LM5140

VDDR_CORE

VCC Voltage Monitor TPS3897A

SENSE_OUT De-Asserted When VDDR_CORE(0.85V) < 0.55V

Test Automation Header

SW Reg 3V3,500mA (TPS62177)

SW Reg 3V3,3A (TPS54334)

3V3 PREREG

PG from TPS62823

EN_3V3 SW Regulator LM5140

PG_0V

PG_3V3

EN_5V0

3V3_5V

Fixed Reg 1V8,3A (TPS62087)

EN

PG

LDO 1V8,1A (TPS74601)

EN

PG

SW Reg 1V2,2A (TPS62097)

EN

PG

SW Reg 0.75V,0.8V/0.85V (TPS62823)

EN

PG

R3

VDDR_CORE

R4

DC-DC Converter 0.85V,1.5A_{no} (TPS82084)

EN

Ren

VPP 1V8,0.5A (TLV75518P)

EN

LDO 2.8V,200mA (TLV70728P)

EN

SW Reg 1V1,2A (TPS62097)

EN

LDO 1.0V,200mA (TLV70710)

EN

SW Reg 2.5V,2A (TPS62097)

EN

LDO 2V5,500mA (TPS73525)

EN

VTT 0.6V,2A (TPS51206)

EN

From GPIO (Disabled by default)

From GPIO (Disabled by default)

VCC3V3_SYS

VCC3V3_TA

Reset Switch

Test Automation Header

POrz

SoC_PORz

VIN_MON_PORz

JTAG_EMU_RESEt

SOC_POWER_MON_PORz

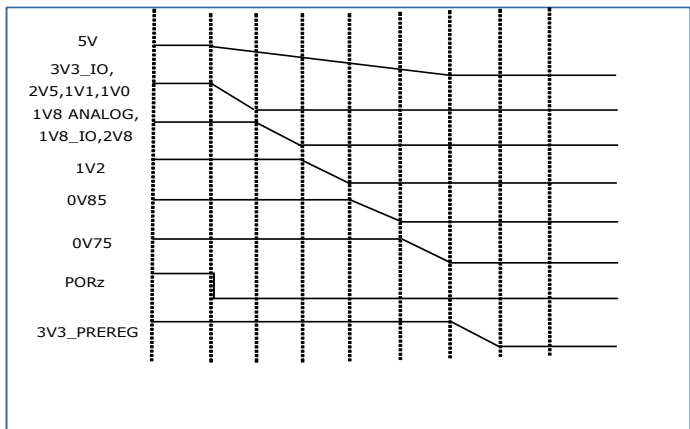
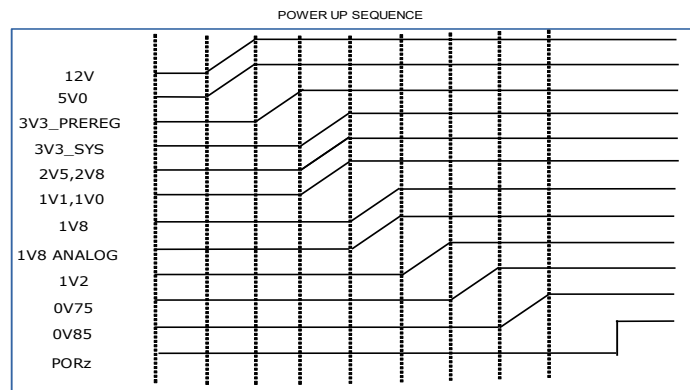
SENSE RESET Voltage Monitor TPS3897A

EN

POWER UP SEQUENCE

POWER DOWN SEQUENCE

If VDD_CORE = 0.75V, 0.8V Mount Ren,R4 & DNI R3
If VDD_CORE =0.85 Mount R3 & DNI Ren,R4



GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPI0_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via OE res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2Interrupt			Interrupt			INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPIO_PCl_e_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN transceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN transceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
18	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPI0_CSn1	OUTPUT	LOW	HIGH
19	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPI0_CS1	INPUT	HIGH	LOW
20	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
21	OLED Display RESET GPIO	GPIO_OLED_RESETh	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
22	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
23	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 01.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
24	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Selection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
25	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
26	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH
27	One GPIO to enable the PCIe Clock generator outputs	CDC_OE1/E4	GP EVM	Clock output enable	IO EXPANDER- P21		OUTPUT	HIGH	HIGH

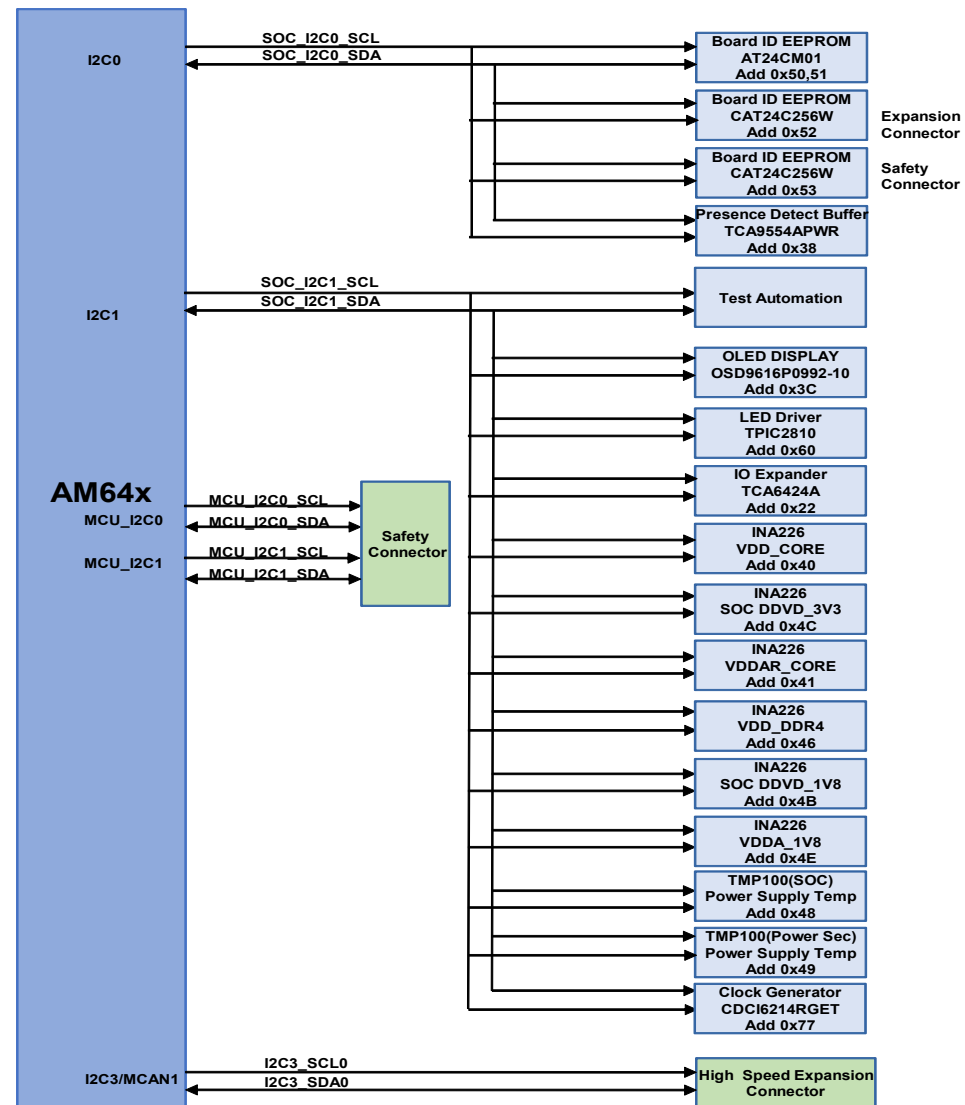
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Title GPIO MAPPING TABLE

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 7 of 40

I2C TREE



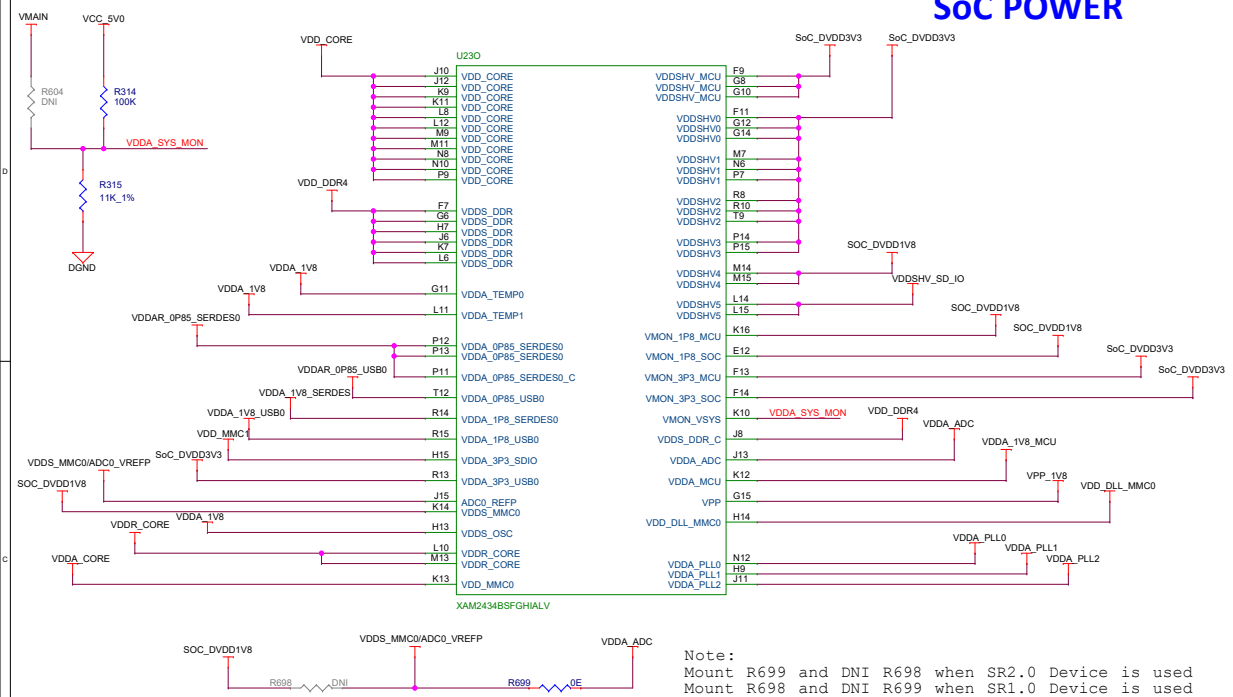
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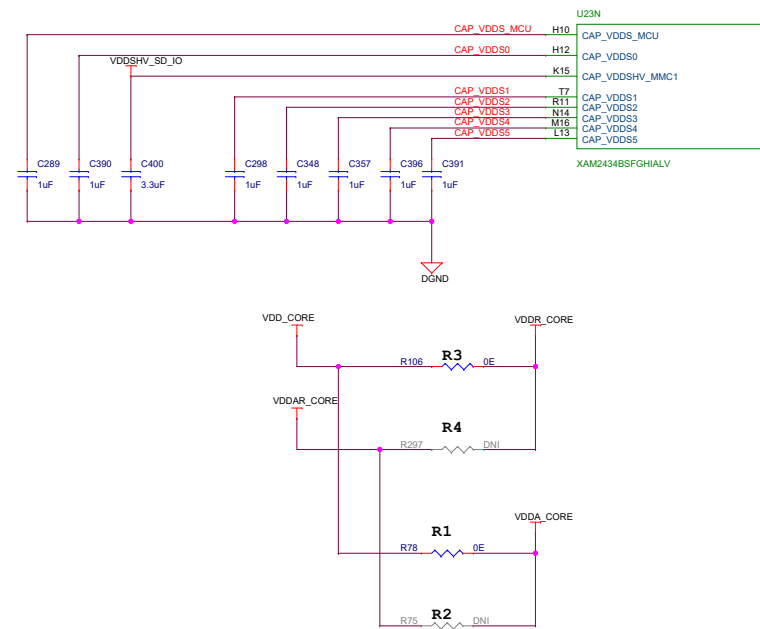
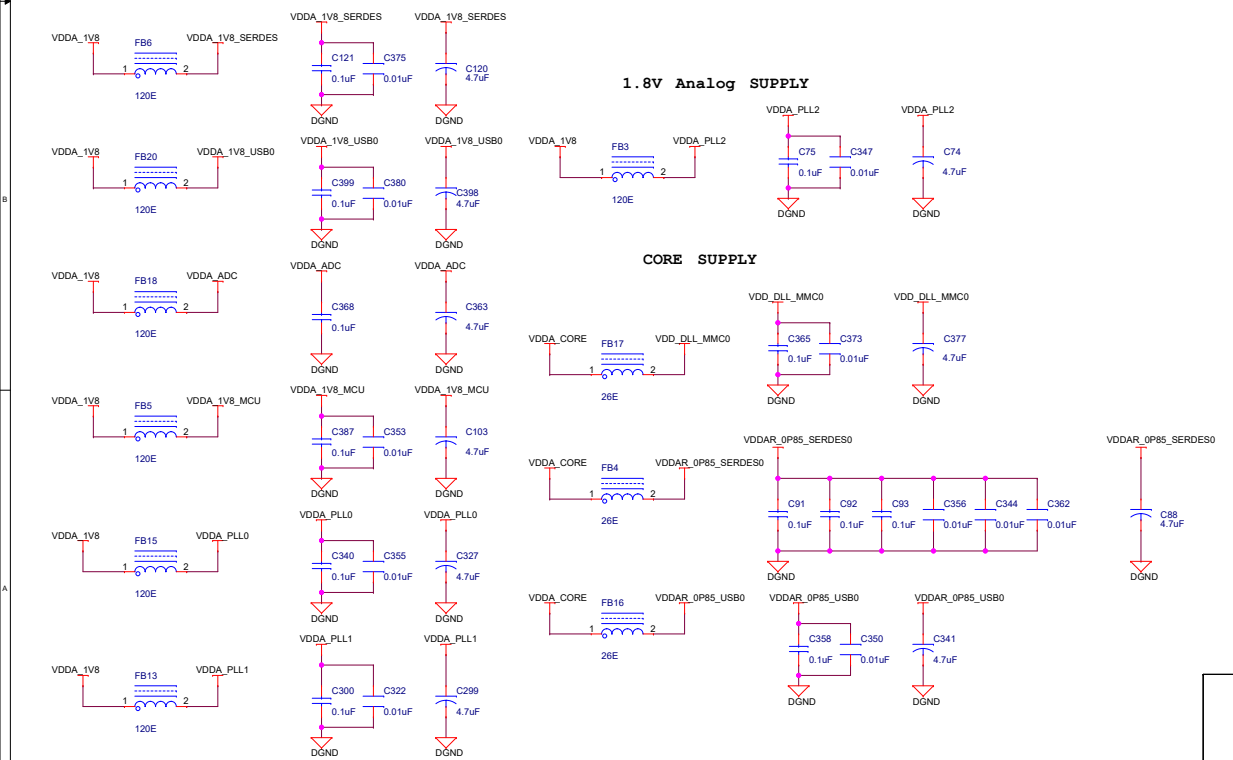
Title I2C TREE

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 8 of 40

SoC POWER

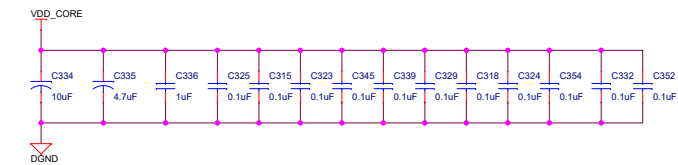


1.8V Analog SUPPLY

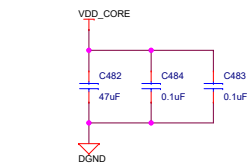


CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE	0.85 VDDR_CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD_CORE & OTHERS	0.85 VDDR_CORE	R1 & R4 INSTALLED
0.85 VDD_CORE,VDDR_CORE&OTHERS	NONE	R1 & R3 INSTALLED

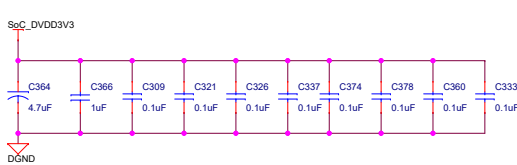
SoC POWER Decaps



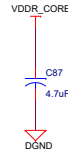
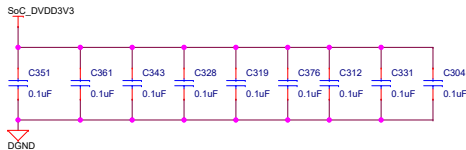
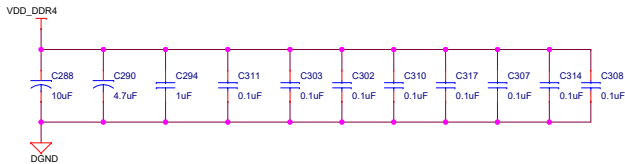
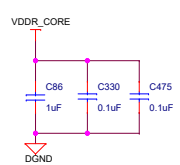
Place one 0.1uF cap near each Pin



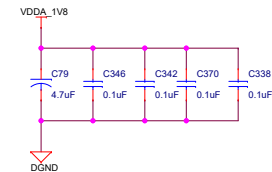
To place after current sense resitor on VDD_CORE plane



Place one 0.1uF cap near each Pin

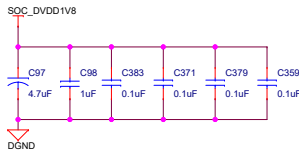
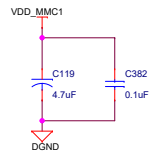


VDD ARRAY CORE

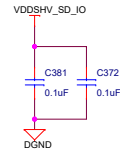


Place one 0.1uF cap near each Pin

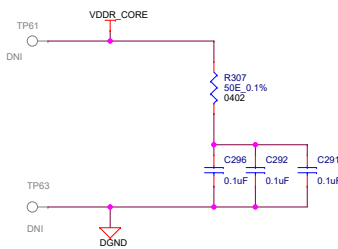
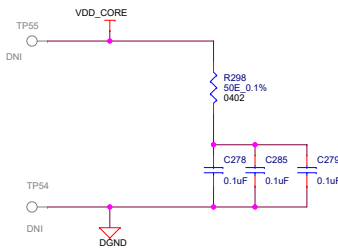
VDDA_3P3_SDIO



Place one 0.1uF cap near each Pin

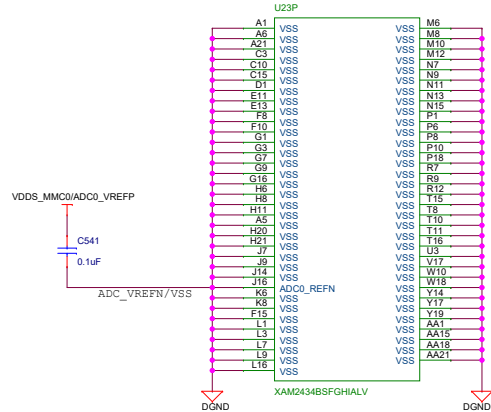


Core & Array Core Supply Kelvin Sensing



SoC POWER - VSS

CAD Note:
Place CAP C541
between pins
J15 and J16



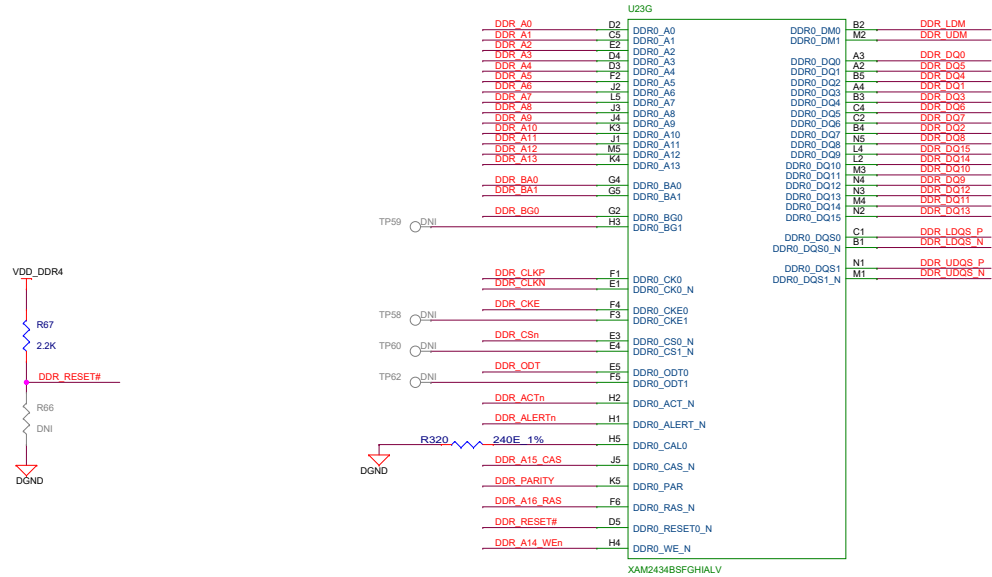
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Title SOC VSS

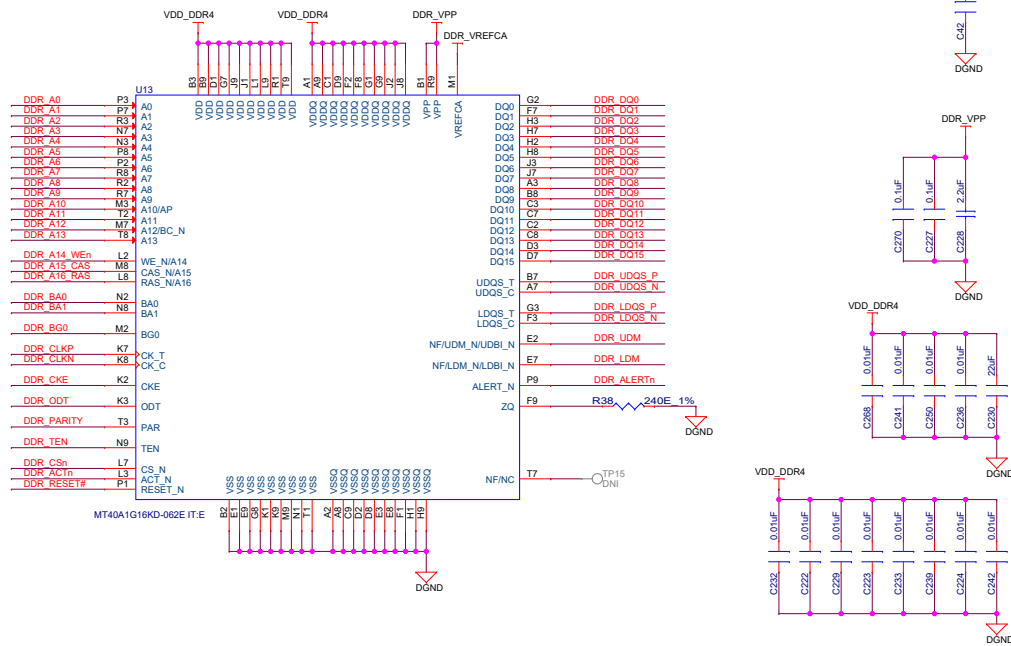
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 11 of 40

SoC DDR INTERFACE

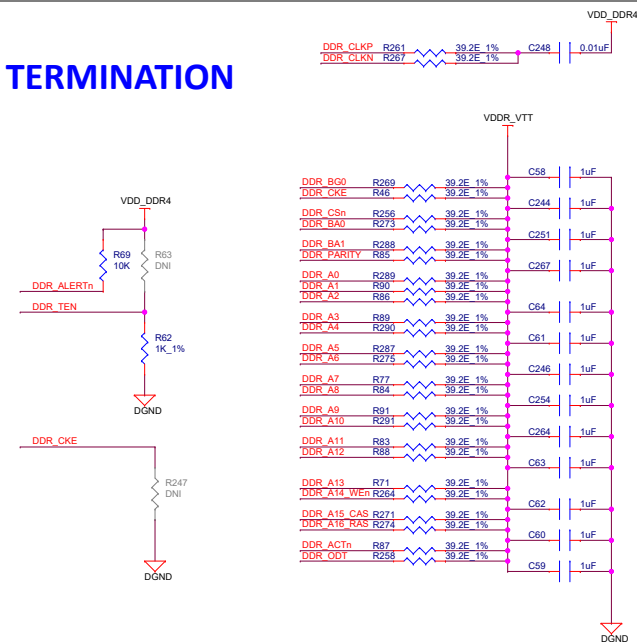


DDR DQ Lines Swapped
With Data Byte

DDR4 DEVICE



DDR TERMINATION



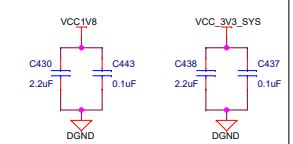
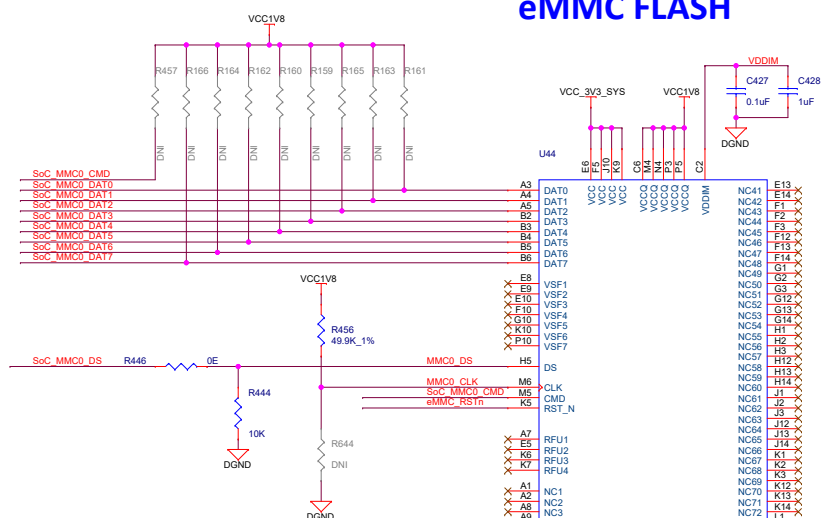
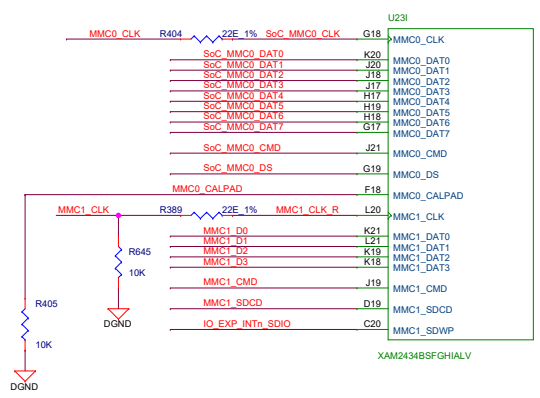
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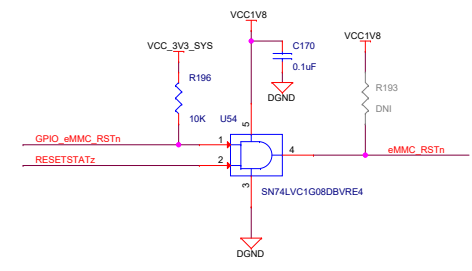
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Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 12 of 40

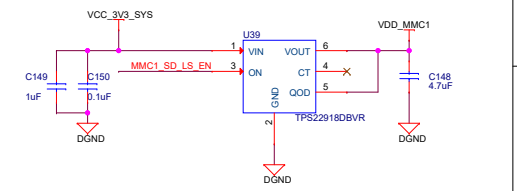
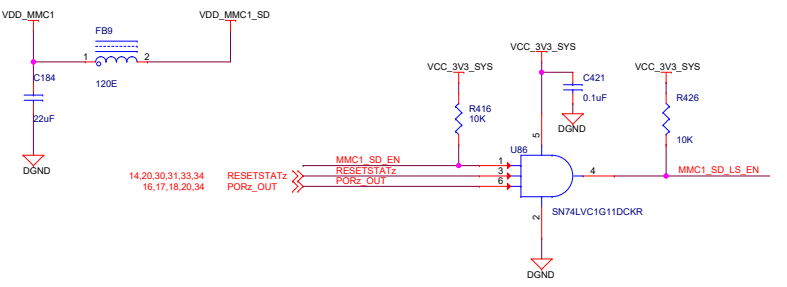
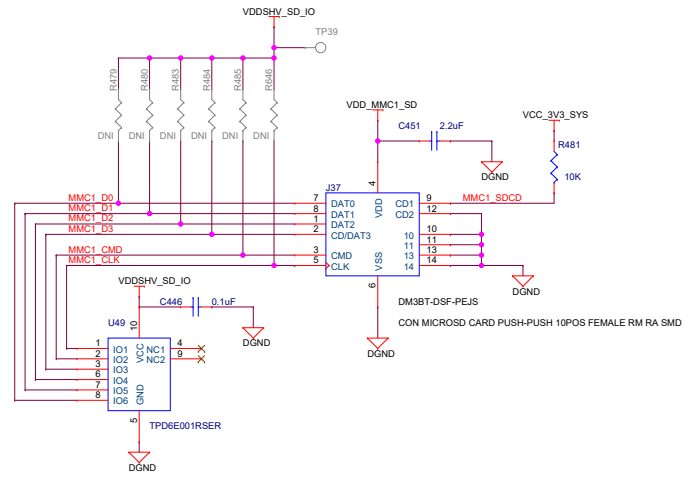
eMMC FLASH



eMMC FLASH RESET



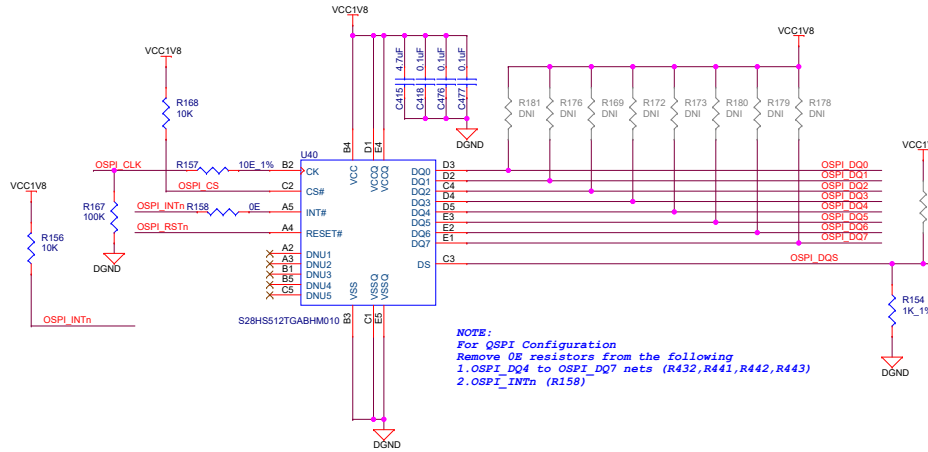
SD CARD INTERFACE



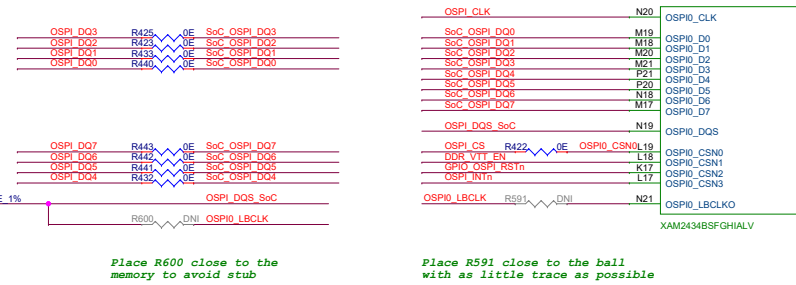
Off Page Connections

From 4	33	IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO
To IO Expander	33	GPIO_eMMC_RSTn	GPIO_eMMC_RSTn
	33	MMC1_SD_EN	MMC1_SD_EN

OSPI FLASH

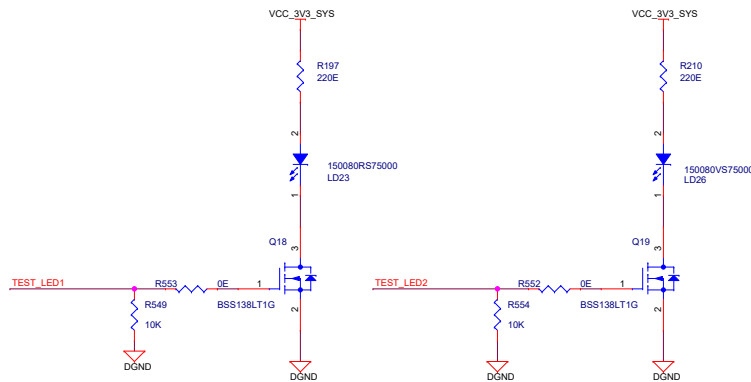


SOC OSPI INTERFACE

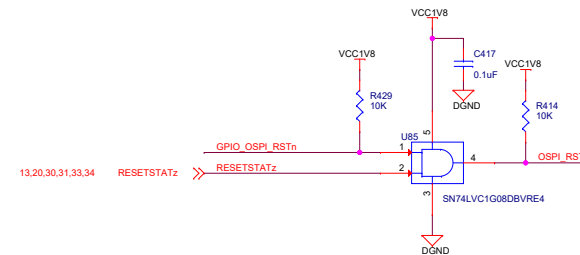


To Route DQS to LBCLK0	To Route DQS to SOC's DQS
Mount R591 & R600	Mount R601 & R592
DNI R601 & R592	DNI R591 & R600

USER TEST LED



OSPI FLASH RESET



Off Page Connections

TEST_LED1	TEST_LED1	33
TEST_LED2	TEST_LED2	34
DDR_VTT_EN	DDR_VTT_EN	33

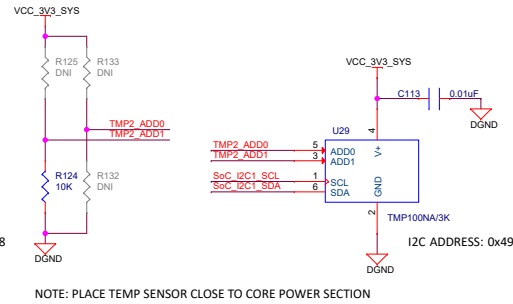
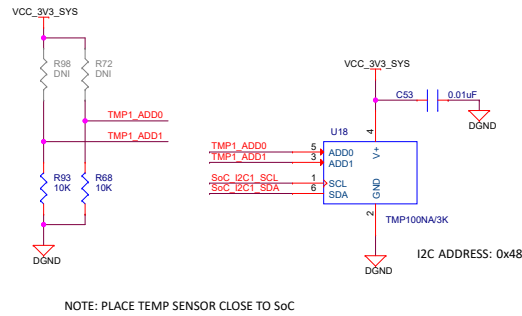
To Level Translator

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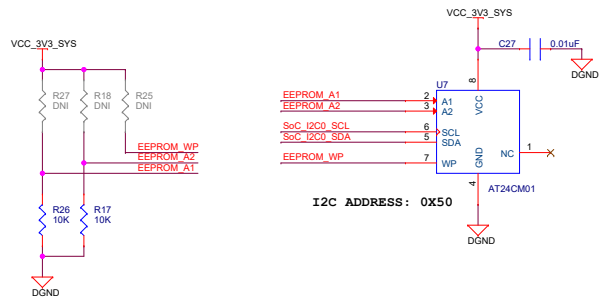
Title		OSPI
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 14 of 40

TEMPERATURE SENSOR

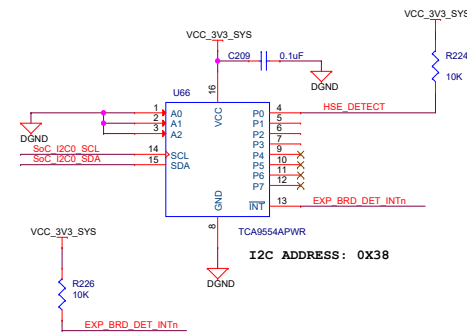


SoC_I2C1_SCL DNI TP25
SoC_I2C1_SDA DNI TP27

BOARD ID EEPROM



BOARD PRESENCE DETECT CIRCUIT



Off Page Connections

HSE_DETECT	←	HSE_DETECT	27
SoC_I2C1_SDA	↔	SoC_I2C1_SDA	19,21,29,30,31,32,33
SoC_I2C1_SCL	↔	SoC_I2C1_SCL	19,21,29,30,31,32,33
SoC_I2C0_SDA	↔	SoC_I2C0_SDA	27,29,33
SoC_I2C0_SCL	↔	SoC_I2C0_SCL	27,29,33

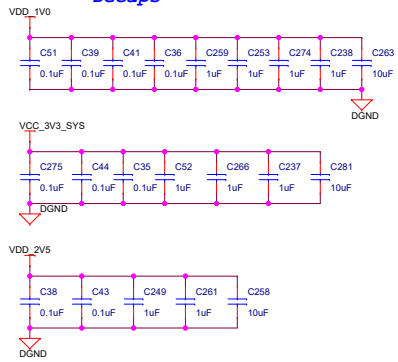
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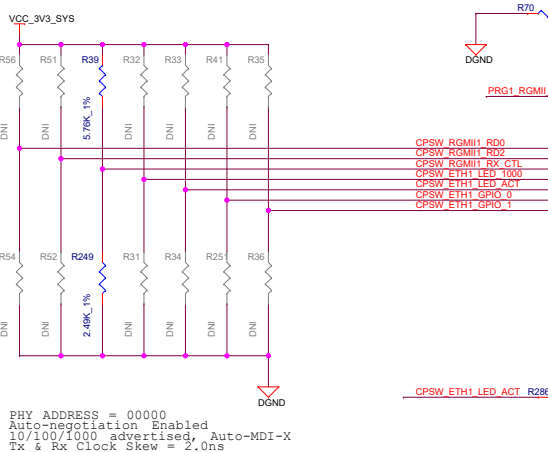
Title EEPROM, PRESENCE DETECTION & TEMP SENSOR

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 15 of 40

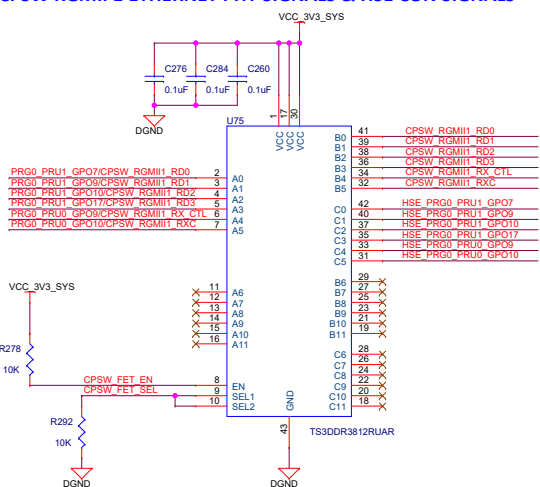
Decaps



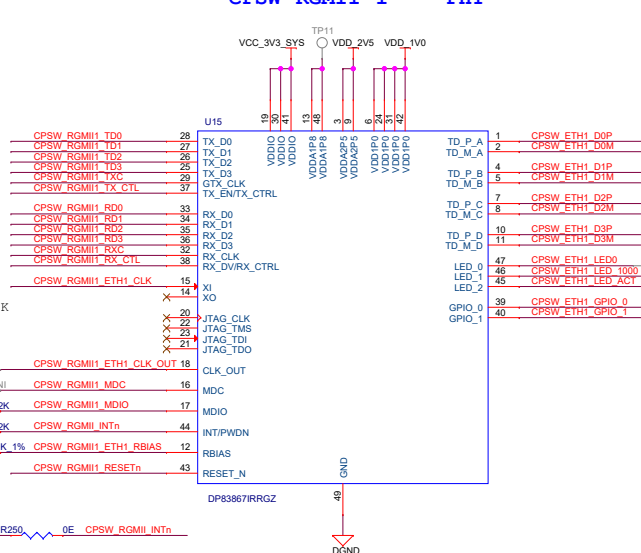
STRAPPING RESISTORS



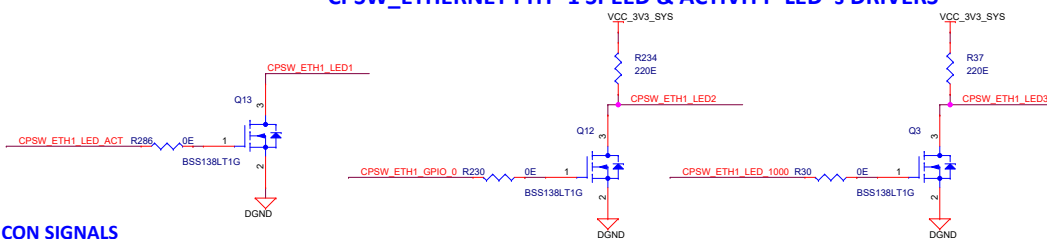
CPSW RGMII 1 ETHERNET PHY SIGNALS & HSE CON SIGNALS



CPSW RGMII 1 - PHY



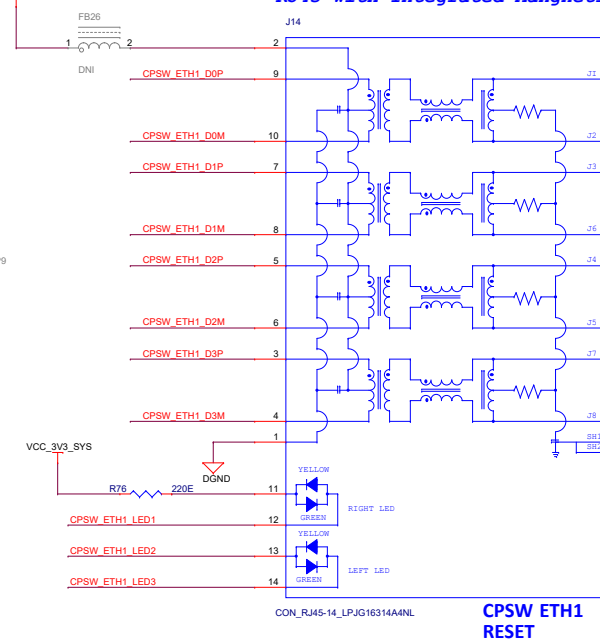
CPSW_ETHERNET PHY- 1 SPEED & ACTIVITY LED 's DRIVERS



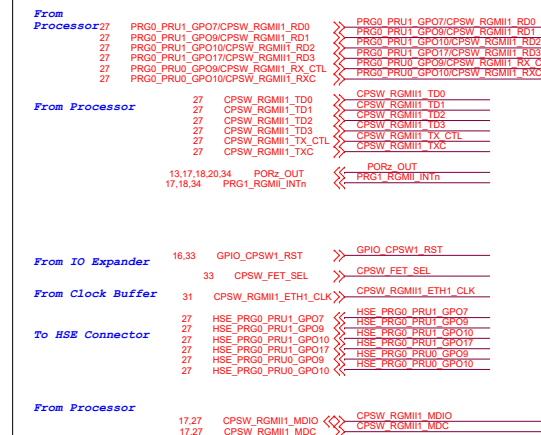
TS3DDR3812RUAR Truth Table

EN	SEL1	SEL2	FUNCTION
L	X	X	A0 to A11, B0 to B11, and C0 to C11 are Hi-Z
H	L	L	A0 to A5 = B0 to B5 and A6 to A11 = B6 to B11
H	L	H	A0 to A5 = B0 to B5 and A6 to A11 = C6 to C11
H	H	L	A0 to A5 = C0 to C5 and A6 to A11 = B6 to B11
H	H	H	A0 to A5 = C0 to C5 and A6 to A11 = C6 to C11

RJ45 with Integrated Magnetics

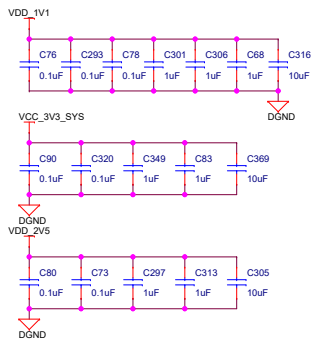


Off Page Connections

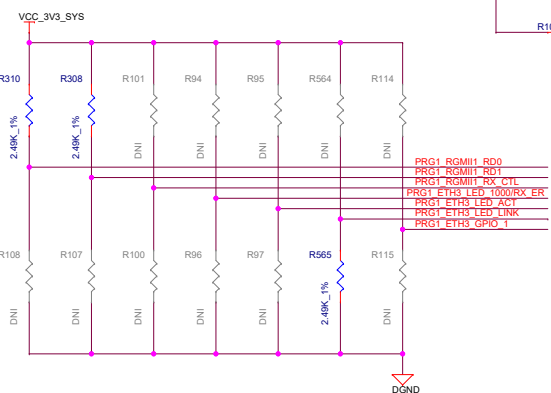


ICSSG1 - RGMII 1

Decaps

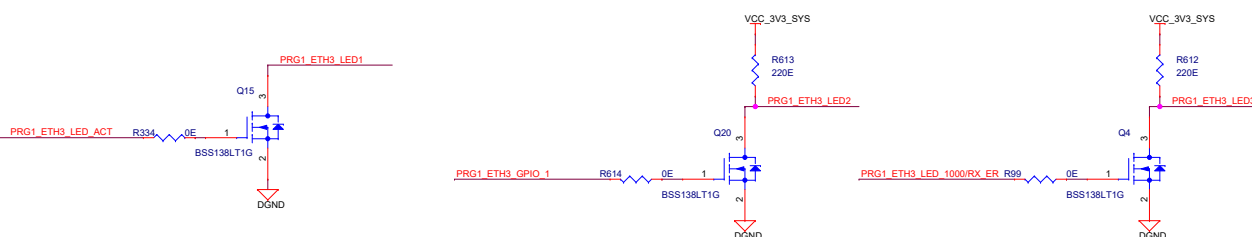


STRAPPING RESISTORS

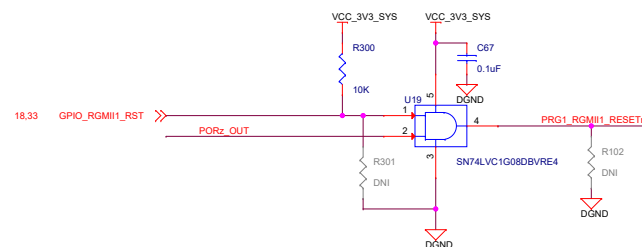


PHY ADDRESS = 01111
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000Base-T/100Base-TX/10Base-T)

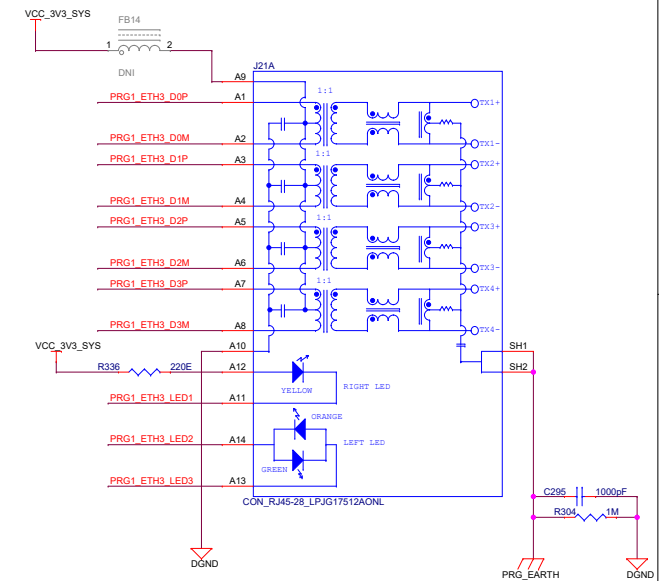
PRG1_ETHERNET - 3 SPEED & ACTIVITY LED's DRIVERS



PRG1 ETH2 RESET



Dual RJ45 CON With Integrated Magnetics



Off Page Connections

To Processor	16,17,34	PRG1_RGMII_INTn	PRG1_RGMII_INTn
	27	PRG1_RGMII_RD0	PRG1_RGMII_RD0
	27	PRG1_RGMII_RD1	PRG1_RGMII_RD1
	27	PRG1_RGMII_RD2	PRG1_RGMII_RD2
	27	PRG1_RGMII_RD3	PRG1_RGMII_RD3
	27	PRG1_RGMII_RXC	PRG1_RGMII_RXC
	27	PRG1_RGMII_RX_CTL	PRG1_RGMII_RX_CTL
13,16,17,20,34	PORz_OUT	PORz_OUT	
	27	PRG1_ETH3_LED_LINK	PRG1_ETH3_LED_LINK
27	PRG1_ETH3_LED_1000RX_ER	PRG1_ETH3_LED_1000RX_ER	
From Processor	27	PRG1_RGMII_TD0	PRG1_RGMII_TD0
	27	PRG1_RGMII_TD1	PRG1_RGMII_TD1
	27	PRG1_RGMII_TD2	PRG1_RGMII_TD2
	27	PRG1_RGMII_TD3	PRG1_RGMII_TD3
	27	PRG1_RGMII_TXC	PRG1_RGMII_TXC
	27	PRG1_RGMII_TX_CTL	PRG1_RGMII_TX_CTL
	27		
From Processor	17,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	17,27	PRG1_MDIO_MDC	PRG1_MDIO_MDC
From IO Expander	18,33	GPIO_RGMII_RST	GPIO_RGMII_RST
	31	PRG1_RGMII_ETH3_CLK	PRG1_RGMII_ETH3_CLK

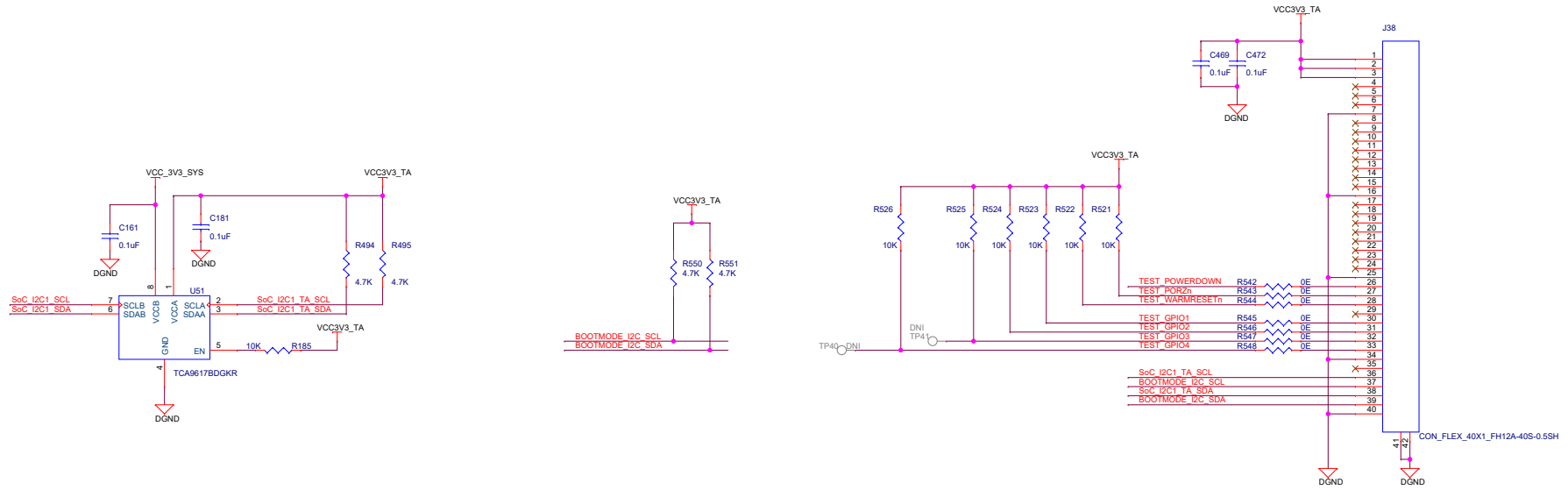
Designed for TI by Mistral Solutions Pvt Ltd



Title		ICSSG2 RGMII_1 ETHERNET PHY	
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev	
C		E2	
Date:	Thursday, August 18, 2022	Sheet	18 of 40

TEST AUTOMATION

40-PIN AUTOMATION HEADER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to I/O Expander to Communicate with SoC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

Off Page Connections

To Processor	15,21,29,30,31,32,33	SoC I2C1 SCL	SoC I2C1 SCL
	15,21,29,30,31,32,33	SoC I2C1 SDA	SoC I2C1 SDA
To Bootmode Buffer	20	BOOTMODE_I2C_SCL	BOOTMODE_I2C_SCL
	20	BOOTMODE_I2C_SDA	BOOTMODE_I2C_SDA
To Debounce Ckt	35	TEST_PORZn	TEST_PORZn
To High Side SW	37	TEST_POWERDOWN	TEST_POWERDOWN
To Debounce Ckt	35	TEST_WARMRESETn	TEST_WARMRESETn
To IO Expander	35	TEST_GPIO1	TEST_GPIO1
To EN Boot Mode Buffer	33	TEST_GPIO2	TEST_GPIO2
To RST Boot Mode Buffer	20	TEST_GPIO3	TEST_GPIO3
	20	TEST_GPIO4	TEST_GPIO4

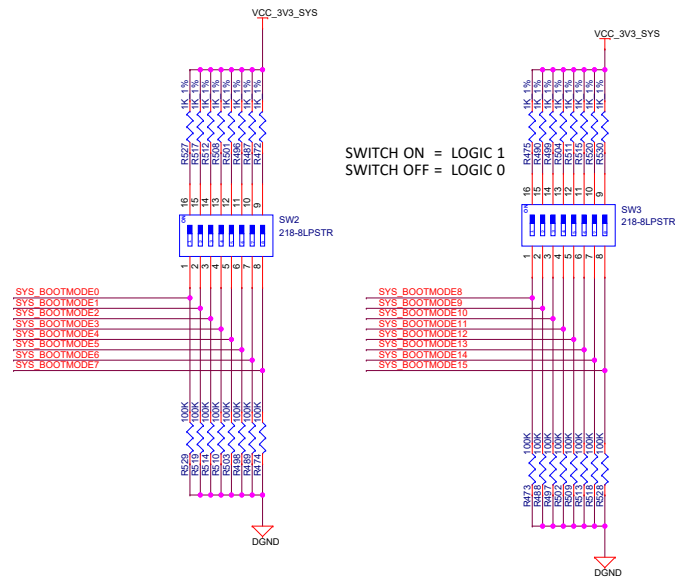
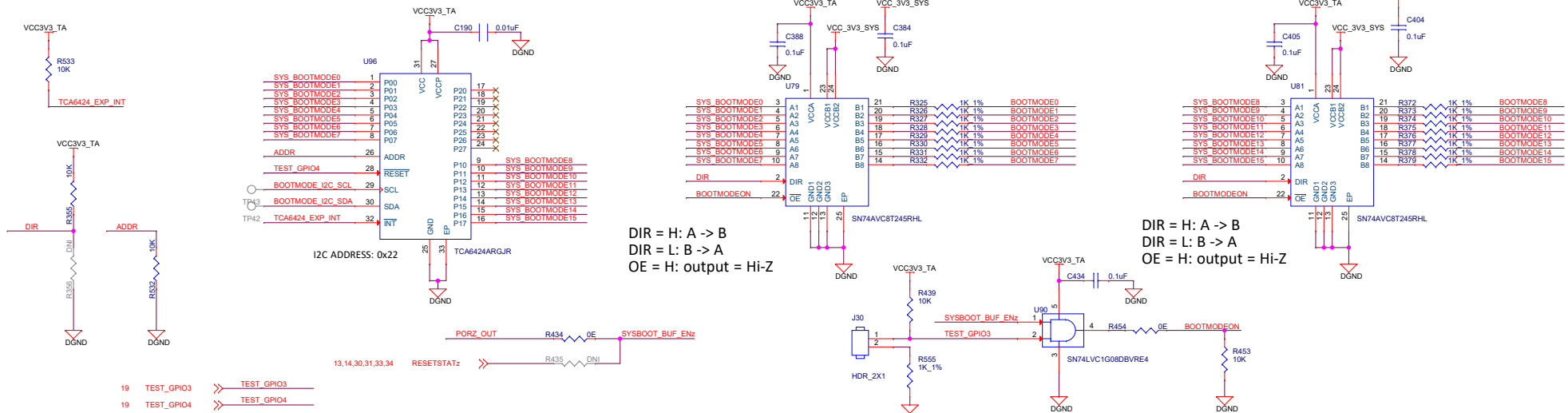
Designed for TI by Mistral Solutions Pvt Ltd



Title TEST AUTOMATION

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 19 of 40

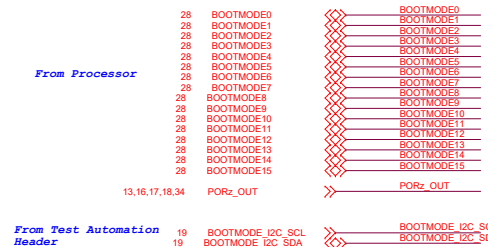
BOOT MODE BUFFER & SWITCHES



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. CPSW Ethernet Slave
5. USB Host
6. USB Device
7. UART
8. Ethernet

Off Page Connections



Designed for TI by Mistral Solutions Pvt Ltd

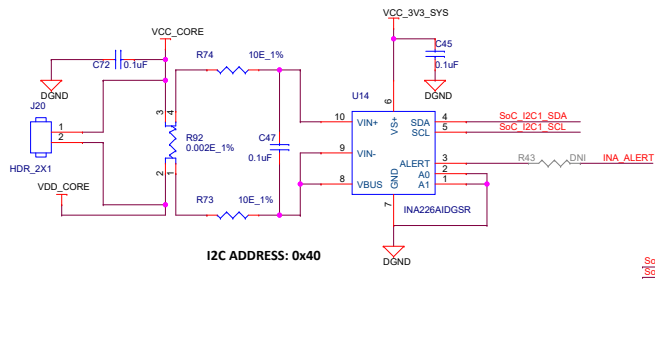


Title BOOT MODE BUFFER & SWITCHES

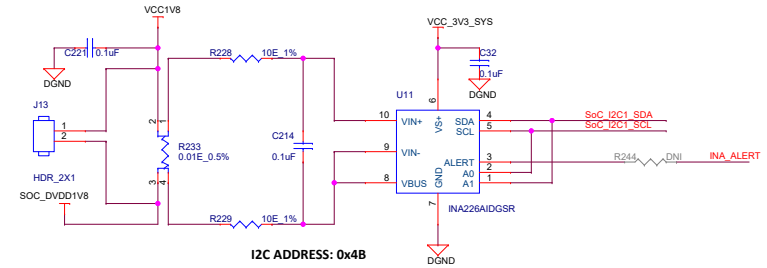
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 20 of 40

CURRENT MONITORING DEVICES

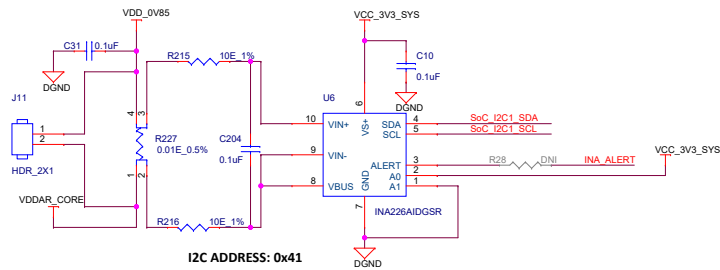
VDD_CORE



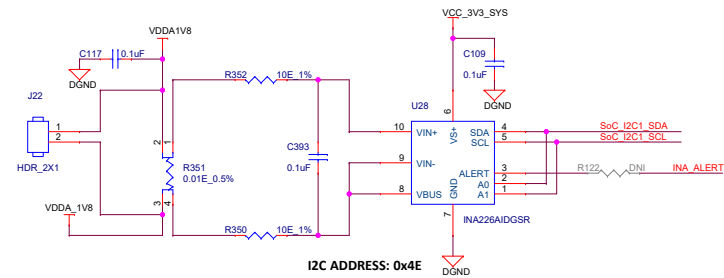
SoC_DVDD1V8



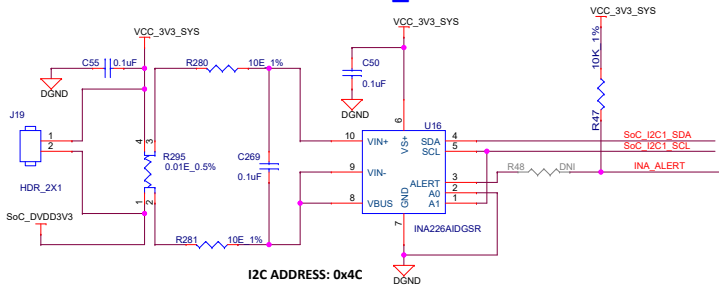
VDDAR_CORE



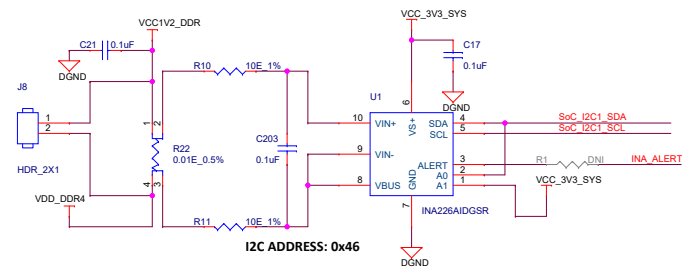
VDDA_1V8



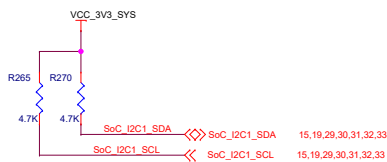
SoC_DVDD3V3



VDD_DDR4



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_OV85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46



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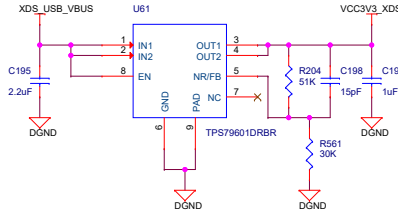
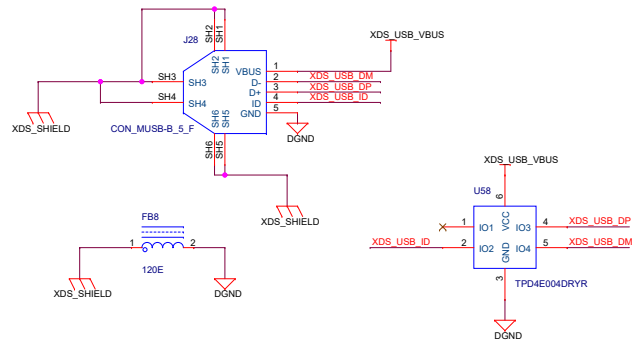


Title CURRENT MONITORING DEVICES

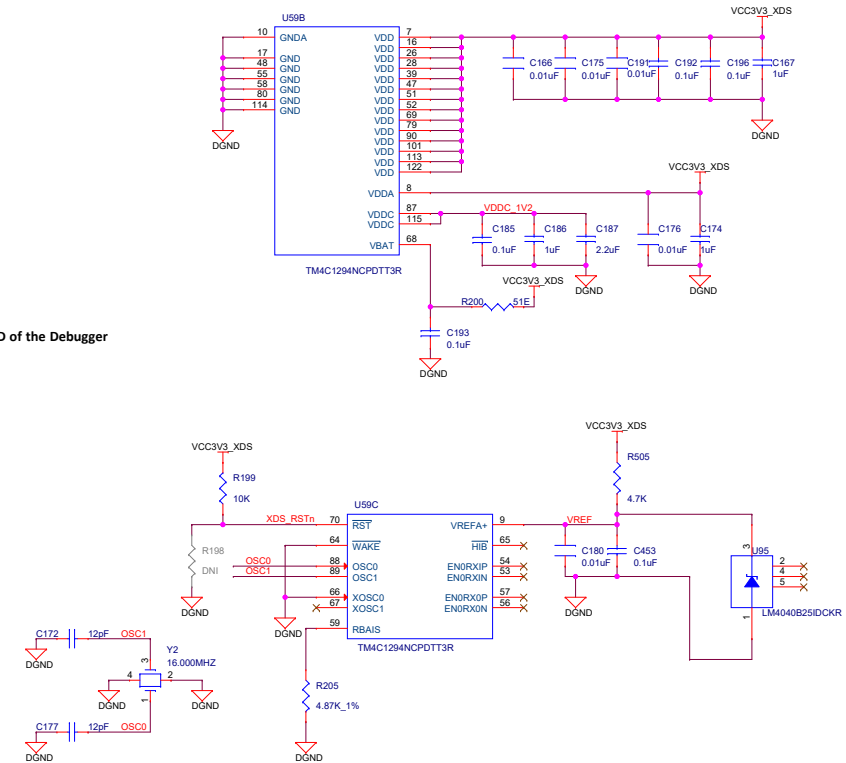
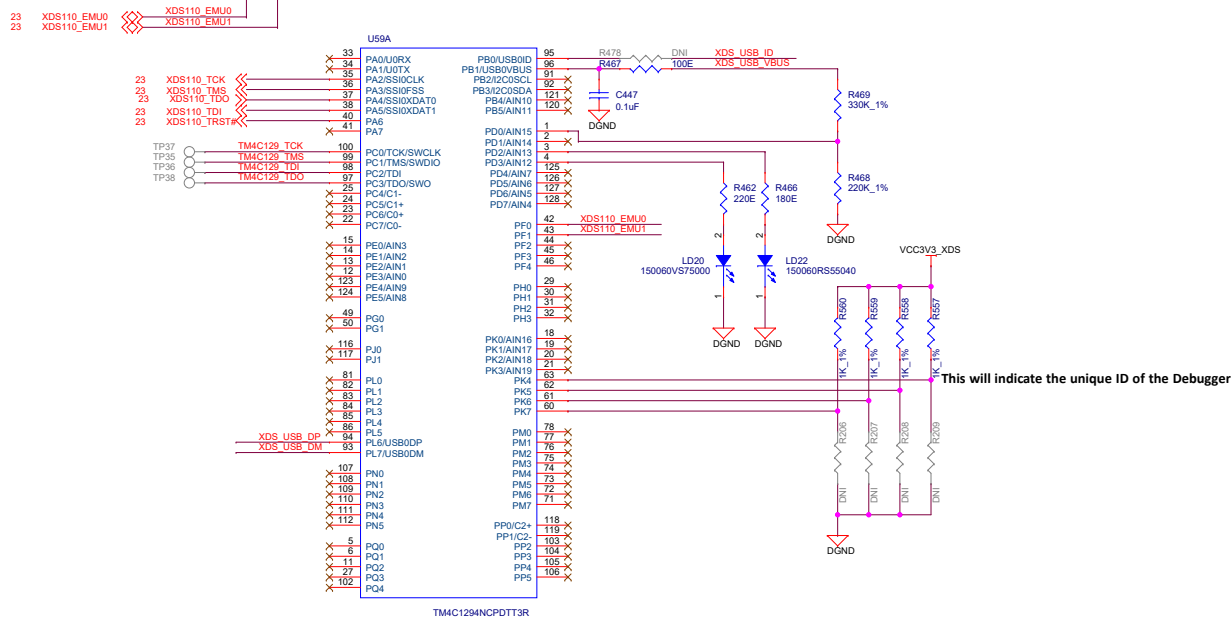
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 21 of 40

USB Connector

XDS110 POWER



XDS110 DEBUGGER



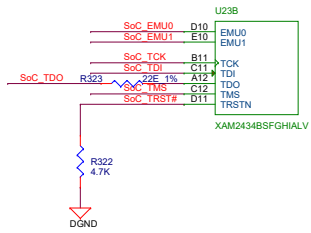
Designed for TI by Mistral Solutions Pvt Ltd



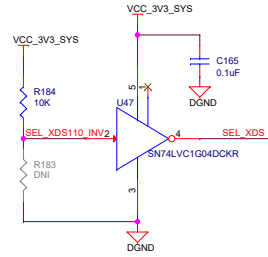
Title XDS110 DEBUGGER

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 22 of 40

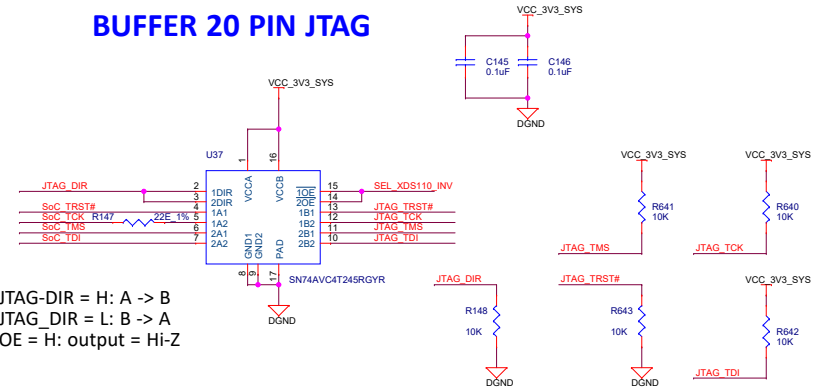
JTAG SoC SECTION



JTAG BUFFER

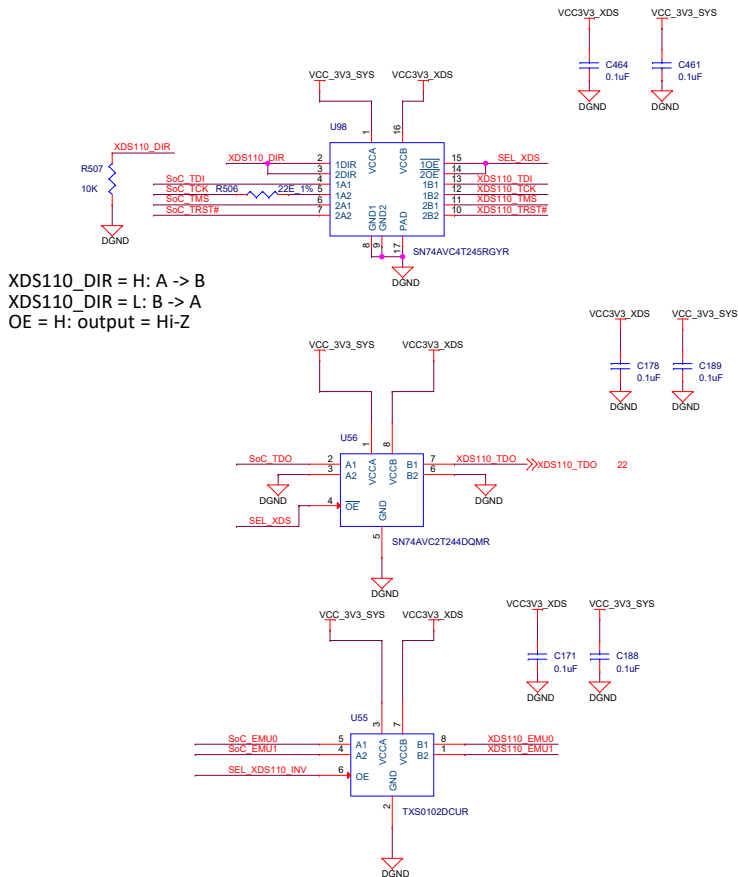


BUFFER 20 PIN JTAG

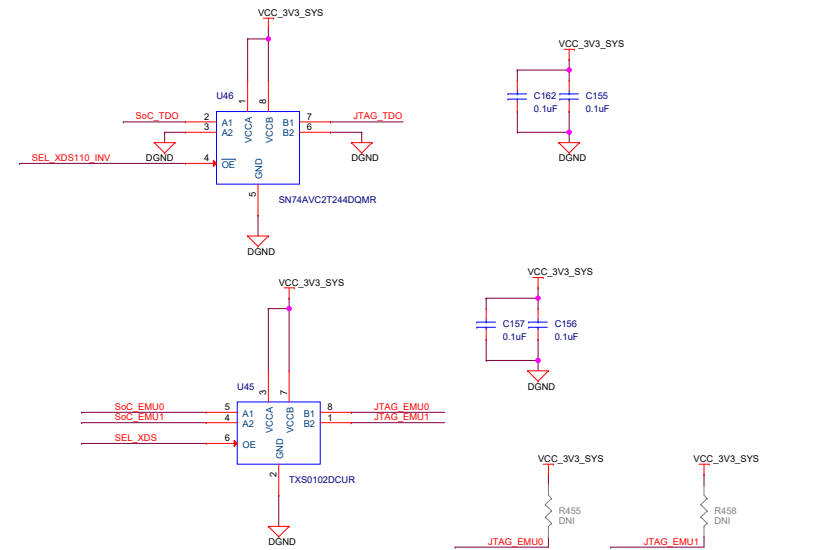


JTAG-DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z

BUFFER XDS110



Placement of Buffers U37, U46, U56 and U98 to be changed to reduce Stub length of the JTAG signals. These buffers need to be placed closer to the cTI-20pin connector -J25



Off Page Connections

From XDS1100 Debugger

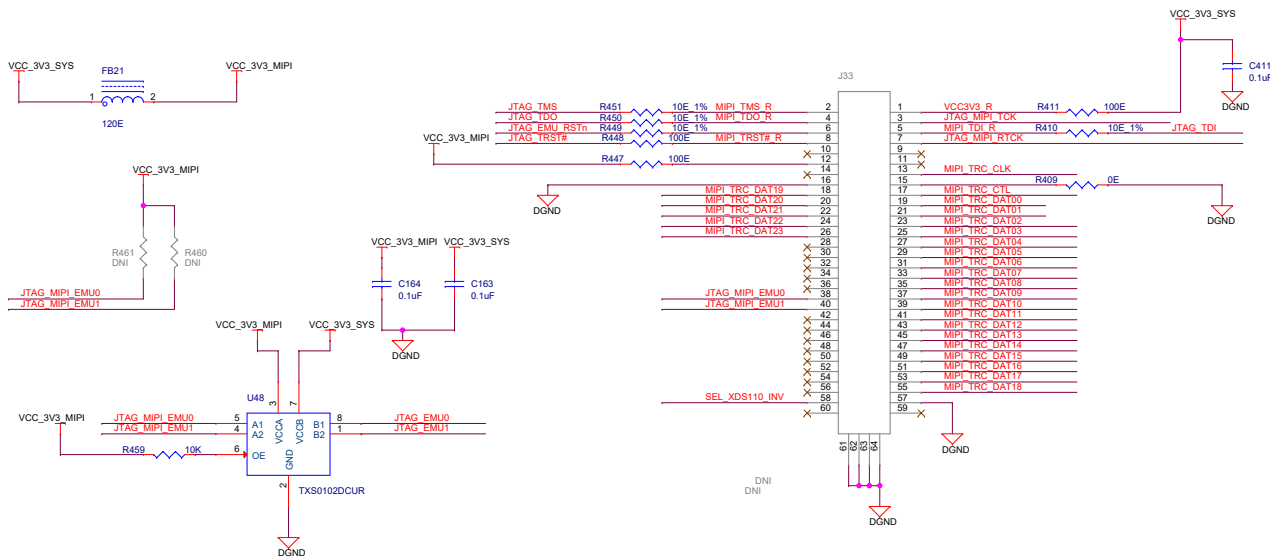
24	SEL_XDS110_INV	SEL_XDS110_INV
24	JTAG_EMU0	JTAG_EMU0
24	JTAG_EMU1	JTAG_EMU1
22	XDS110_TDI	XDS110_TCK
22	XDS110_TCK	XDS110_TMS
22	XDS110_TMS	XDS110_TRST#
22	XDS110_TRST#	JTAG_TDI
24	JTAG_TDI	JTAG_TCK
24	JTAG_TCK	JTAG_TMS
24	JTAG_TMS	JTAG_TRST#
24	JTAG_TRST#	XDS110_EMU0
22	XDS110_EMU0	XDS110_EMU1

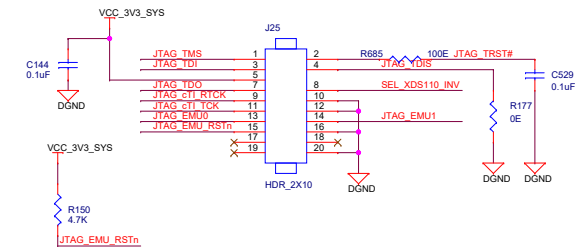
Designed for TI by Mistral Solutions Pvt Ltd

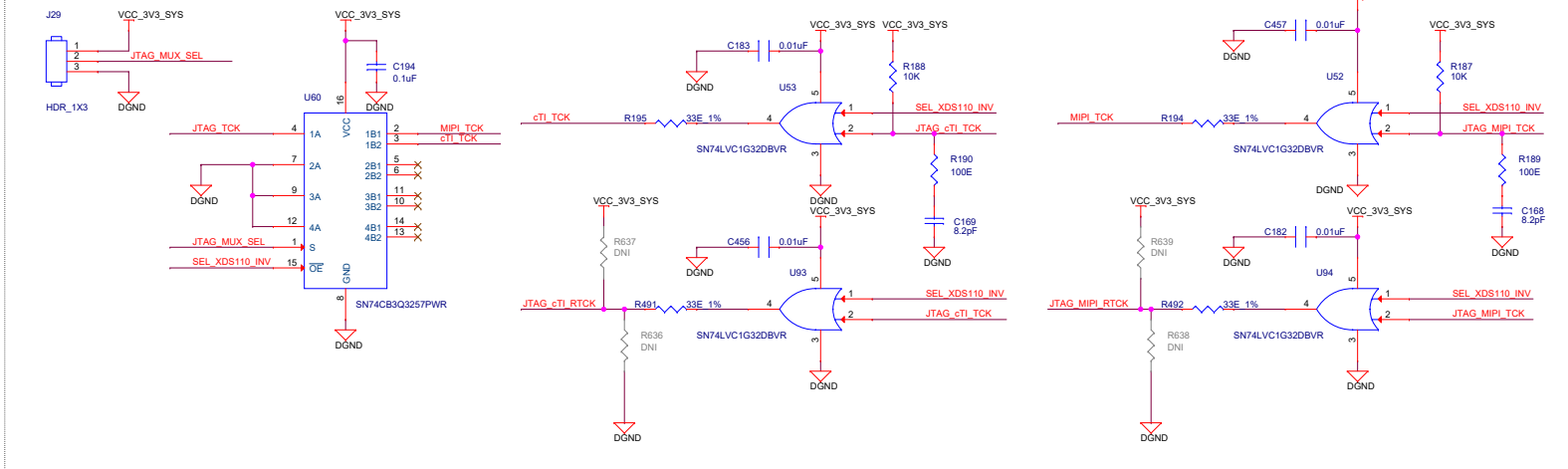


Title JTAG BUFFER

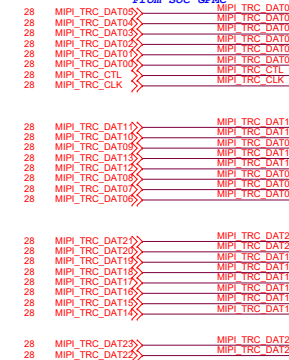
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 23 of 40











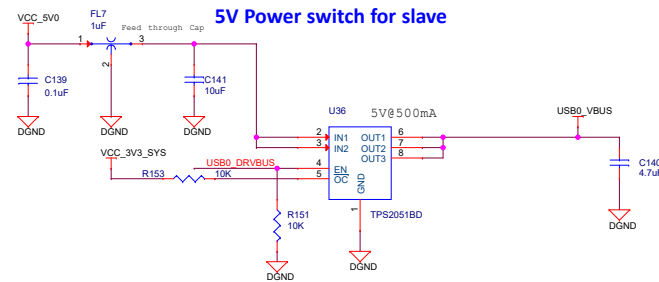
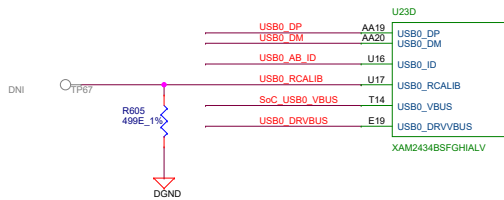
Designed for TI by Mistral Solutions Pvt Ltd



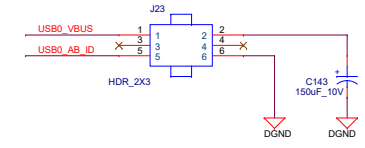
Title MIPI 60 PIN CONNECTOR

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 24 of 40

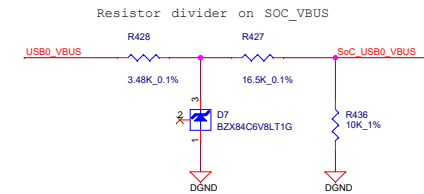
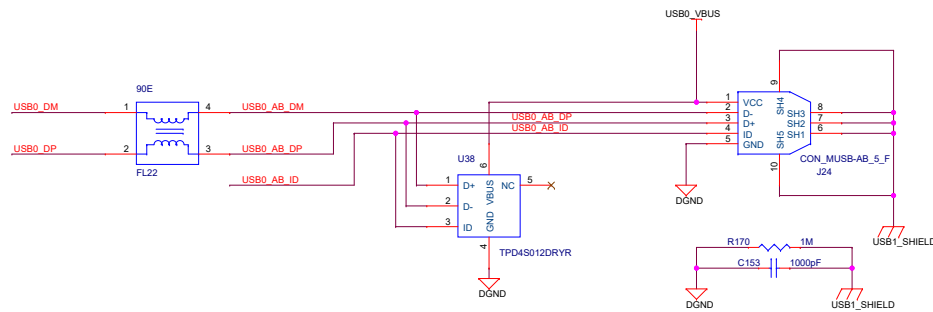
USB 2.0 INTERFACE



2X3 header to enable bulk capacitance on USB0_VBUS in host mode and to ground USB0_AB_ID pin, if a non standard cable is used



Micro USB 2.0 AB Connector



Designed for TI by Mistral Solutions Pvt Ltd



Title USB 2.0 INTERFACE

Size	Variant Name = PROC101C(005) TMD6343EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 25 of 40

[illegible][illegible]

The schematic diagram illustrates the FT4232H-L module, which is a USB-to-UART bridge. The central component is the FT4232H-L IC, which is connected to various power and signal pins. The power pins include VCC_1V8_FT4232, VCC_3V3_FT4232, and VPLL_3V3_FT4232. The signal pins include FT4232_USB_DM, FT4232_USB_DP, FT4232_REF, FT4232_RESET, FT4232_EECS, FT4232_EECLK, FT4232_EEDATA, FT4232_OSCI, FT4232_ OSCO, FT4232_TEST, FT4232_PWREN, and FT4232_SUSPEND. The IC is also connected to various external components, including capacitors (C411, C412, C413, C423, C442, C420, C419, C440, C418, C439, C433, C422, C425), resistors (R175, R464), and a crystal (Y3). The IC is also connected to various external components, including capacitors (C411, C412, C413, C423, C442, C420, C419, C440, C418, C439, C433, C422, C425), resistors (R175, R464), and a crystal (Y3).

The image displays three circuit diagrams for the SN74AVC4T245RSVR transceiver, showing different pin configurations for UART communication. Each diagram includes a 4-pin header (U84) and a 16-pin header (U88).

Diagram 1 (Left): Shows the configuration for SOC MAIN UART0 TX 3V3, SOC MAIN UART0 RTS 3V3, SOC MAIN UART0 RX 3V3, and SOC MAIN UART0 CTS 3V3. The transceiver is connected to VCC_3V3_SYS and VCC_3V3_FT4232. The 4-pin header is connected to VCC_3V3_SYS (pin 1), GND (pin 2), and two other pins (pins 3 and 4). The 16-pin header is connected to VCC_3V3_SYS (pin 1), GND (pin 2), and various signal lines (pins 3-16).

Diagram 2 (Middle): Shows the configuration for SOC MAIN UART1 TX 3V3, SOC MAIN UART1 RX 3V3, SOC MAIN UART1 RTS 3V3, and SOC MAIN UART1 CTS 3V3. The transceiver is connected to VCC_3V3_SYS and VCC_3V3_FT4232. The 4-pin header is connected to VCC_3V3_SYS (pin 1), GND (pin 2), and two other pins (pins 3 and 4). The 16-pin header is connected to VCC_3V3_SYS (pin 1), GND (pin 2), and various signal lines (pins 3-16).

Diagram 3 (Right): Shows the configuration for MCU UART0 TX 3V3, MCU UART0 RX 3V3, MCU UART0 RTS 3V3, and MCU UART0 CTS 3V3. The transceiver is connected to VCC_3V3_SYS and VCC_3V3_FT4232. The 4-pin header is connected to VCC_3V3_SYS (pin 1), GND (pin 2), and two other pins (pins 3 and 4). The 16-pin header is connected to VCC_3V3_SYS (pin 1), GND (pin 2), and various signal lines (pins 3-16).

The schematic shows the connection of an EEPROM chip (93LC46B) to the FT4232 module. The VCC pin (pin 8) is connected to VCC_3V3_FT4232 through a 0.1µF capacitor (C445). The GND pin (pin 7) is connected to DGNDD. The DI pin (pin 3) is connected to FT4232_DO through a 2.2K resistor (R192). The EEDATA pin (pin 4) is connected to FT4232_DO. The CLK pin (pin 2) is connected to FT4232_EECLK. The CS pin (pin 1) is connected to FT4232_EECS. The chip is also connected to pins 6, 7, and NC2.

SOC_MAIN_UART0_RX_3V3	SOC_MAIN_UART0_RX_3V3	29
SOC_MAIN_UART0_TX_3V3	SOC_MAIN_UART0_TX_3V3	29
SOC_MAIN_UART0_RTS_3V3	SOC_MAIN_UART0_RTS_3V3	29
SOC_MAIN_UART0_CTS_3V3	SOC_MAIN_UART0_CTS_3V3	29
MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	34
MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	34
MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	34
MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	34
SOC_MAIN_UART1_RX_3V3	SOC_MAIN_UART1_RX_3V3	29
SOC_MAIN_UART1_TX_3V3	SOC_MAIN_UART1_TX_3V3	29
SOC_MAIN_UART1_RTS_3V3	SOC_MAIN_UART1_RTS_3V3	29
SOC_MAIN_UART1_CTS_3V3	SOC_MAIN_UART1_CTS_3V3	29



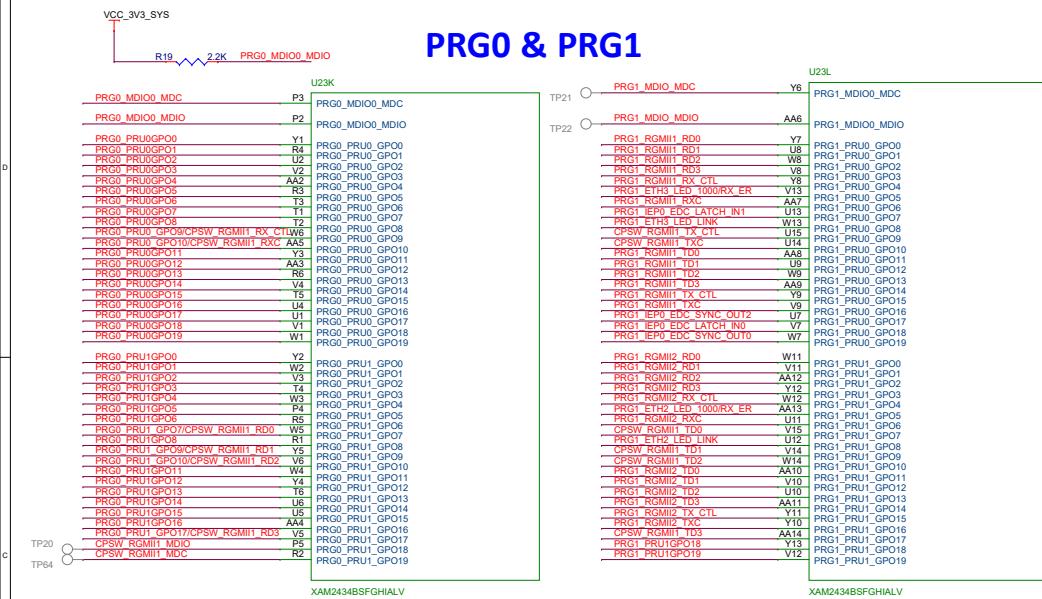
TEXAS
INSTRUMENTS



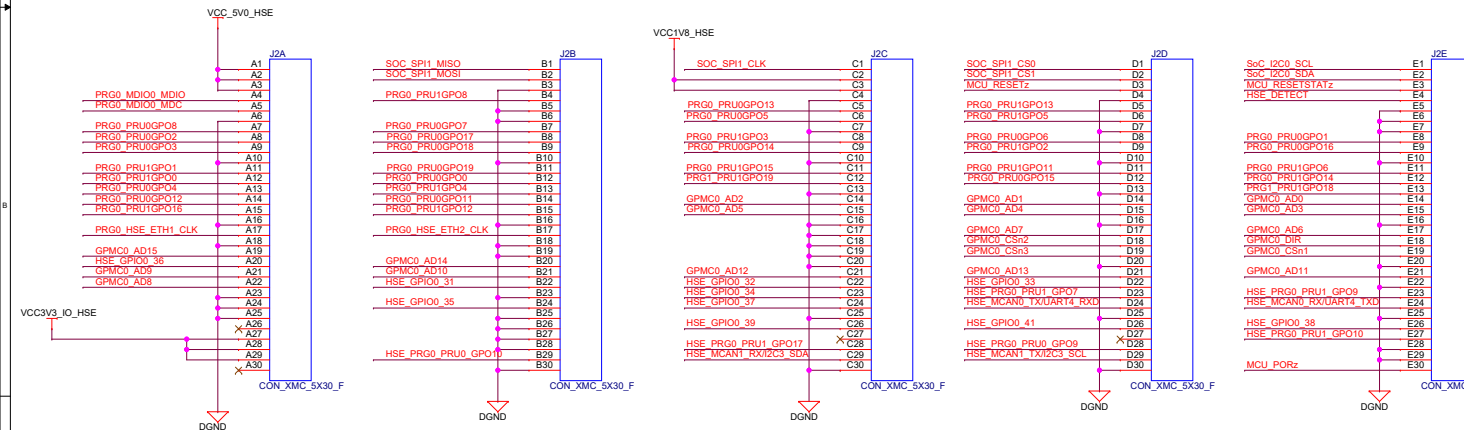
Size	Variant Name = PROC101C(005) TMSD243EVM	
C		
Date:	Thursday, August 18, 2022	Sheet

Rev
E2
40

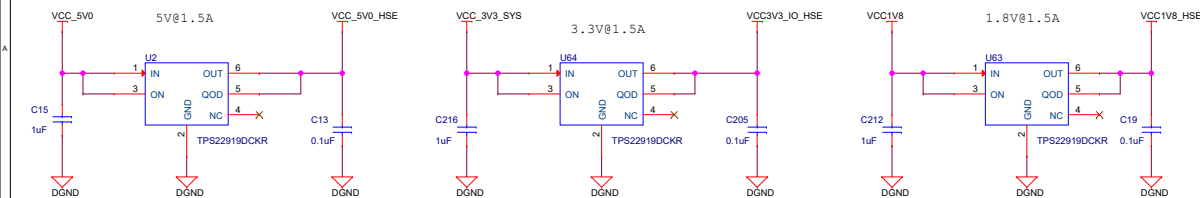
PRG0 & PRG1



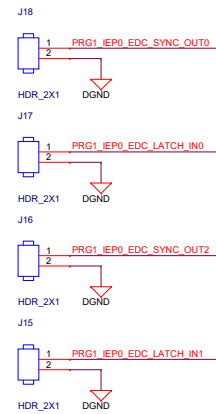
HIGH SPEED EXPANSION CONNECTOR



HSE CONNECTOR LOAD SWITCHES



SYNC TP



Off Page Connections

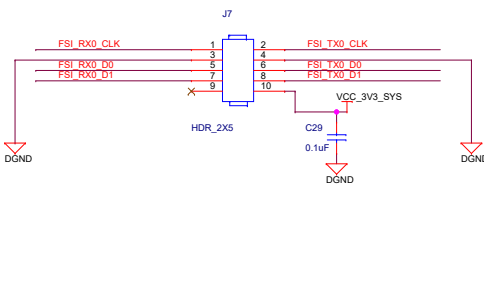
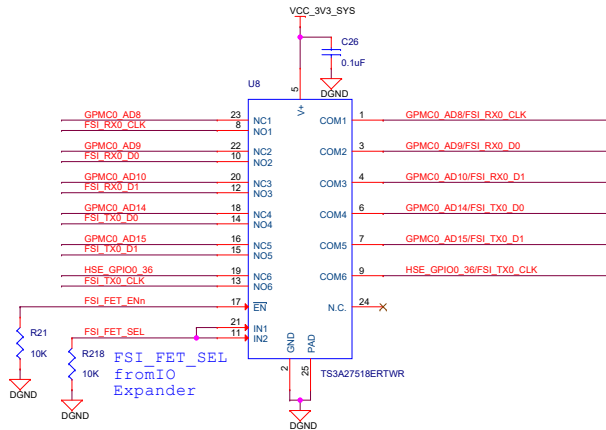
To Presence Detect Buffer	15	HSE_DETECT	<<<	HSE_DETECT
From Processor GPMC	28	GPMC0_CSn1	<<<	GPMC0_CSn1
	28	GPMC0_CSn2	<<<	GPMC0_CSn2
	28	GPMC0_CSn3	<<<	GPMC0_CSn3
	28	GPMC0_DIR	<<<	GPMC0_DIR
From FSI mux	28	GPMC0_A08	<<<	GPMC0_A08
	28	GPMC0_A09	<<<	GPMC0_A09
	28	GPMC0_A10	<<<	GPMC0_A10
	28	GPMC0_A11	<<<	GPMC0_A11
	28	GPMC0_A15	<<<	GPMC0_A15
	28	HSE_GPI00_36	<<<	HSE_GPI00_36
From Processor GPMC resistor muxed with MIP1	28	GPMC0_A00	<<<	GPMC0_A00
	28	GPMC0_A01	<<<	GPMC0_A01
	28	GPMC0_A02	<<<	GPMC0_A02
	28	GPMC0_A03	<<<	GPMC0_A03
	28	GPMC0_A04	<<<	GPMC0_A04
	28	GPMC0_A05	<<<	GPMC0_A05
	28	GPMC0_A06	<<<	GPMC0_A06
	28	GPMC0_A07	<<<	GPMC0_A07
	28	GPMC0_A11	<<<	GPMC0_A11
	28	GPMC0_A12	<<<	GPMC0_A12
	28	GPMC0_A13	<<<	GPMC0_A13
	28	HSE_GPI00_30	<<<	HSE_GPI00_30
	28	HSE_GPI00_33	<<<	HSE_GPI00_33
	28	HSE_GPI00_34	<<<	HSE_GPI00_34
	28	HSE_GPI00_35	<<<	HSE_GPI00_35
	28	HSE_GPI00_36	<<<	HSE_GPI00_36
	28	HSE_GPI00_37	<<<	HSE_GPI00_37
	28	HSE_GPI00_38	<<<	HSE_GPI00_38
	28	HSE_GPI00_39	<<<	HSE_GPI00_39
	28	HSE_GPI00_40	<<<	HSE_GPI00_40
From Processor	34	MCU_PORz	<<<	MCU_PORz
	34,35	MCU_RESEtZ	<<<	MCU_RESEtZ
	34	MCU_RESEtZtAtz	<<<	MCU_RESEtZtAtz
	29	HSE_MCAN0_RXUART4_TX0	<<<	HSE_MCAN0_RXUART4_TX0
	29	HSE_MCAN0_TXUART4_RX0	<<<	HSE_MCAN0_TXUART4_RX0
	29	HSE_MCAN1_TXt2C3_SCL	<<<	HSE_MCAN1_TXt2C3_SCL
	29	HSE_MCAN1_TXt2C3_SCL	<<<	HSE_MCAN1_TXt2C3_SCL
	29	SOC_SP1_CLK	<<<	SOC_SP1_CLK
	29	SOC_SP1_M0S0	<<<	SOC_SP1_M0S0
	29	SOC_SP1_M0S1	<<<	SOC_SP1_M0S1
	29	SOC_SP1_MISO	<<<	SOC_SP1_MISO
	29	SOC_SP1_CS1	<<<	SOC_SP1_CS1
	15,29,33	Soc_I2C0_SCL	<<<	Soc_I2C0_SCL
	15,29,33	Soc_I2C0_SDA	<<<	Soc_I2C0_SDA
From clock Buffer	31	PRG0_HSE_ETH1_CLK	<<<	PRG0_HSE_ETH1_CLK
	31	PRG0_HSE_ETH2_CLK	<<<	PRG0_HSE_ETH2_CLK
To and from ICSSG1 RGMI1 2 Ethernet PHY	17	PRG1_RGMI1_R0	<<<	PRG1_RGMI1_R0
	17	PRG1_RGMI1_RD1	<<<	PRG1_RGMI1_RD1
	17	PRG1_RGMI1_RD2	<<<	PRG1_RGMI1_RD2
	17	PRG1_RGMI1_RXC	<<<	PRG1_RGMI1_RXC
	17	PRG1_RGMI1_RX_CTL	<<<	PRG1_RGMI1_RX_CTL
	17	PRG1_ETH2_LED_1000RX_ER	<<<	PRG1_ETH2_LED_1000RX_ER
	17	PRG1_RGMI1_T00	<<<	PRG1_RGMI1_T00
	17	PRG1_RGMI1_T01	<<<	PRG1_RGMI1_T01
	17	PRG1_ETH3_LED_LINK	<<<	PRG1_ETH3_LED_LINK
	17	PRG1_ETH2_LED_LINK	<<<	PRG1_ETH2_LED_LINK
	17	PRG1_RGMI1_R0	<<<	PRG1_RGMI1_R0
	17	PRG1_RGMI1_RD1	<<<	PRG1_RGMI1_RD1
	17	PRG1_RGMI1_RD2	<<<	PRG1_RGMI1_RD2
	17	PRG1_RGMI1_R03	<<<	PRG1_RGMI1_R03
	17	PRG1_RGMI1_RXC	<<<	PRG1_RGMI1_RXC
	17	PRG1_RGMI1_RX_CTL	<<<	PRG1_RGMI1_RX_CTL
	17	PRG1_ETH3_LED_1000RX_ER	<<<	PRG1_ETH3_LED_1000RX_ER
	17,18	PRG1_MDIO_MDIO	<<<	PRG1_MDIO_MDIO
	17,18	PRG1_MDIO_MDC	<<<	PRG1_MDIO_MDC
To and from ICSSG2 RGMI1 1 Ethernet PHY	18	PRG1_ETH3_LED_LINK	<<<	PRG1_ETH3_LED_LINK
	18	PRG1_ETH2_LED_LINK	<<<	PRG1_ETH2_LED_LINK
	18	PRG1_RGMI1_R0	<<<	PRG1_RGMI1_R0
	18	PRG1_RGMI1_RD1	<<<	PRG1_RGMI1_RD1
	18	PRG1_RGMI1_RD2	<<<	PRG1_RGMI1_RD2
	18	PRG1_RGMI1_R03	<<<	PRG1_RGMI1_R03
	18	PRG1_RGMI1_RXC	<<<	PRG1_RGMI1_RXC
	18	PRG1_RGMI1_RX_CTL	<<<	PRG1_RGMI1_RX_CTL
	18	PRG1_ETH3_LED_1000RX_ER	<<<	PRG1_ETH3_LED_1000RX_ER
From MUX To HSE	16	HSE_PRG0_PRU1_GPO7	<<<	HSE_PRG0_PRU1_GPO7
	16	HSE_PRG0_PRU1_GPO9	<<<	HSE_PRG0_PRU1_GPO9
	16	HSE_PRG0_PRU1_GPO10	<<<	HSE_PRG0_PRU1_GPO10
	16	HSE_PRG0_PRU1_GPO17	<<<	HSE_PRG0_PRU1_GPO17
	16	HSE_PRG0_PRU1_GPO19	<<<	HSE_PRG0_PRU1_GPO19
	16	HSE_PRG0_PRU1_GPO10	<<<	HSE_PRG0_PRU1_GPO10
	16,17	CPSW_RGMI1_MDIO	<<<	CPSW_RGMI1_MDIO
	16,17	CPSW_RGMI1_MDC	<<<	CPSW_RGMI1_MDC
To MUX From Soc	16	PRG0_PRU1_GPO7/CPSW_RGMI1_R0	<<<	PRG0_PRU1_GPO7/CPSW_RGMI1_R0
	16	PRG0_PRU1_GPO9/CPSW_RGMI1_R0	<<<	PRG0_PRU1_GPO9/CPSW_RGMI1_R0
	16	PRG0_PRU1_GPO10/CPSW_RGMI1_R0	<<<	PRG0_PRU1_GPO10/CPSW_RGMI1_R0
	16	PRG0_PRU1_GPO17/CPSW_RGMI1_R0	<<<	PRG0_PRU1_GPO17/CPSW_RGMI1_R0
	16	PRG0_PRU1_GPO19/CPSW_RGMI1_R0	<<<	PRG0_PRU1_GPO19/CPSW_RGMI1_R0
	16	PRG0_PRU1_GPO10/CPSW_RGMI1_RXC	<<<	PRG0_PRU1_GPO10/CPSW_RGMI1_RXC
From PSW RGMI1 1 PHY	16	CPSW_RGMI1_T00	<<<	CPSW_RGMI1_T00
	16	CPSW_RGMI1_T01	<<<	CPSW_RGMI1_T01
	16	CPSW_RGMI1_T02	<<<	CPSW_RGMI1_T02
	16	CPSW_RGMI1_T03	<<<	CPSW_RGMI1_T03
	16	CPSW_RGMI1_TX_CTL	<<<	CPSW_RGMI1_TX_CTL
	16	CPSW_RGMI1_RX_CTL	<<<	CPSW_RGMI1_RX_CTL

GPMC



GPMC TO FSI & HSE CONNECTOR

FSI CONNECTOR



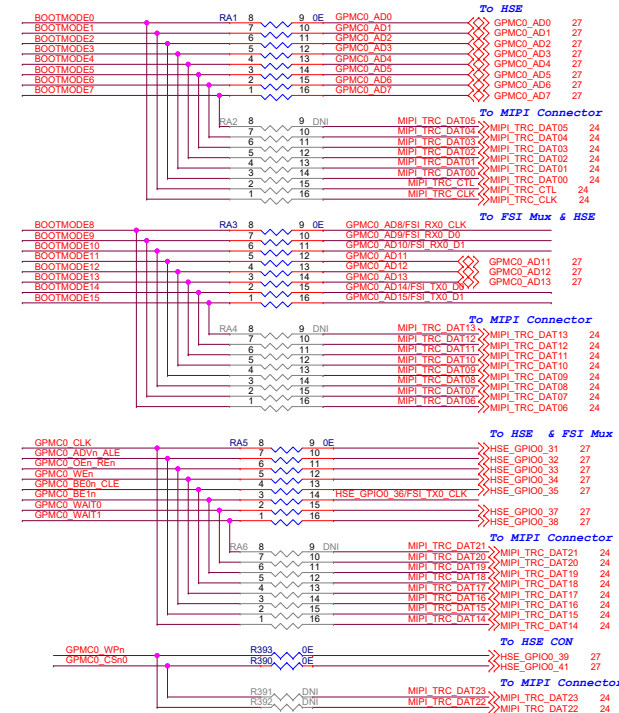
TS3A27518ERTWR Truth Table

EN#	IN1	IN2	NC1/2/3 TO COM1/2/3 & COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM1/2/3 & COM1/2/3 TO NC4/5/6	NO1/2/3 TO COM1/2/3 & COM1/2/3 TO NO1/2/3	NC4/5/6 TO COM1/2/3 & COM1/2/3 TO NC4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

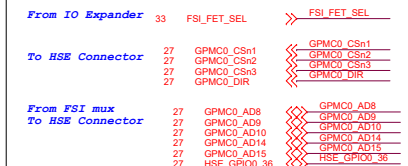
0- Ohm Res MUX between HSE Connector and TRACE Functionality

-For HSE Connector RA1, RA3, RA5, R393 & R390 Should be installed and RA2, RA4, RA6, R391& R392 Should be DNI'd.

-For TRACE RA2, RA4, RA6, R391& R392 Should be installed and RA1, RA3, RA5, R393 & R390 Should be DNI'd.



Off Page Connections

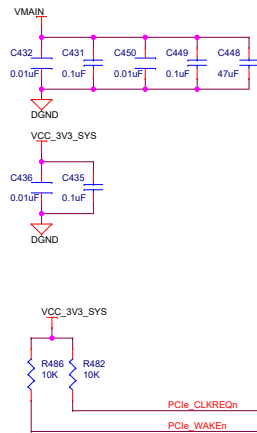


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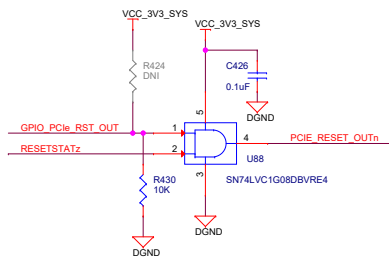


Title		GPMC	
Size	Variant Name = PROC101C(005) TMD5243EVM		Rev
C			E2
Date:	Thursday, August 18, 2022	Sheet	28 of 40

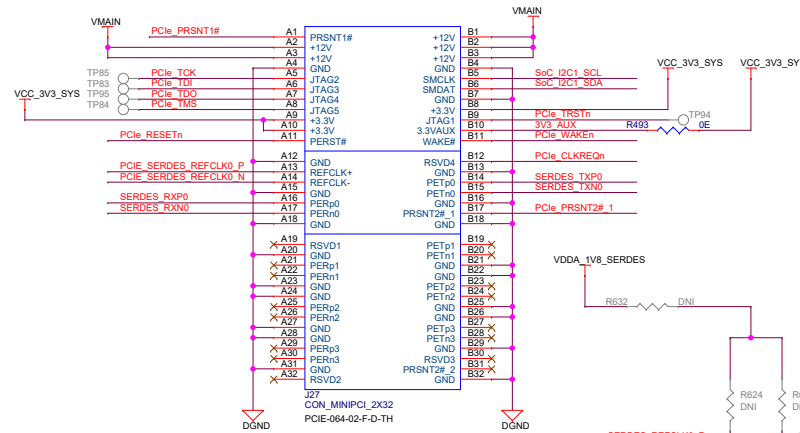
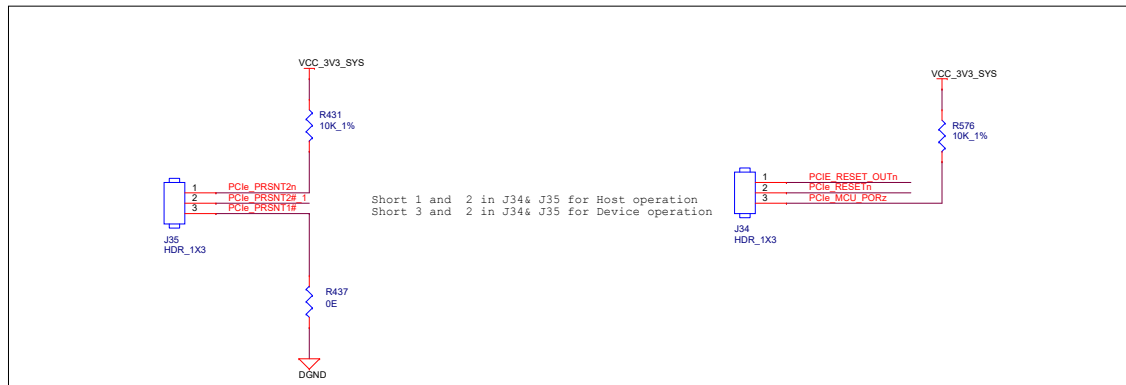
x4 Lane PCIe Connector



PCIe Reset

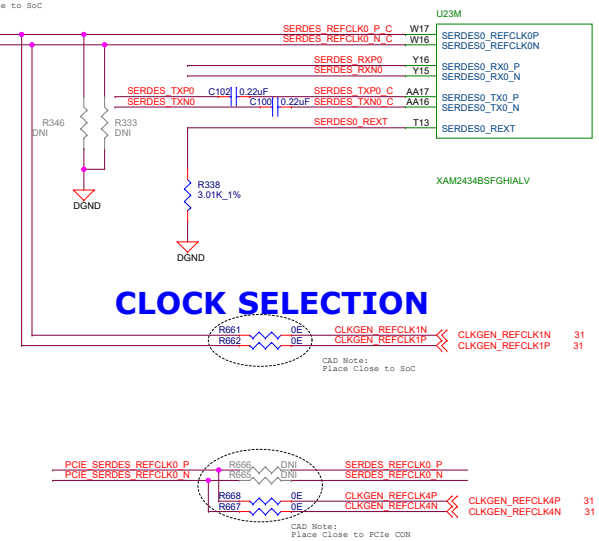


RC OR EP MODE SELECTION



Note:
R679 , R680 Mounted with 0E Resistor when PCIe REFCLK is in no Re-biasing Mode.
R679 , R680 to be replaced with 100nf CAP 0402 package when PCIe REFCLK is in Re-biasing Mode.

CLOCK SELECTION



Off Page Connections

PCIe MCU_PORz	PCIe_MCU_PORz	34
GPIO_PClk_RST_OUT	GPIO_PClk_RST_OUT	33
RESETSTATz	RESETSTATz	13,14,20,31,33,34
SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,31,32,33
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,31,32,33

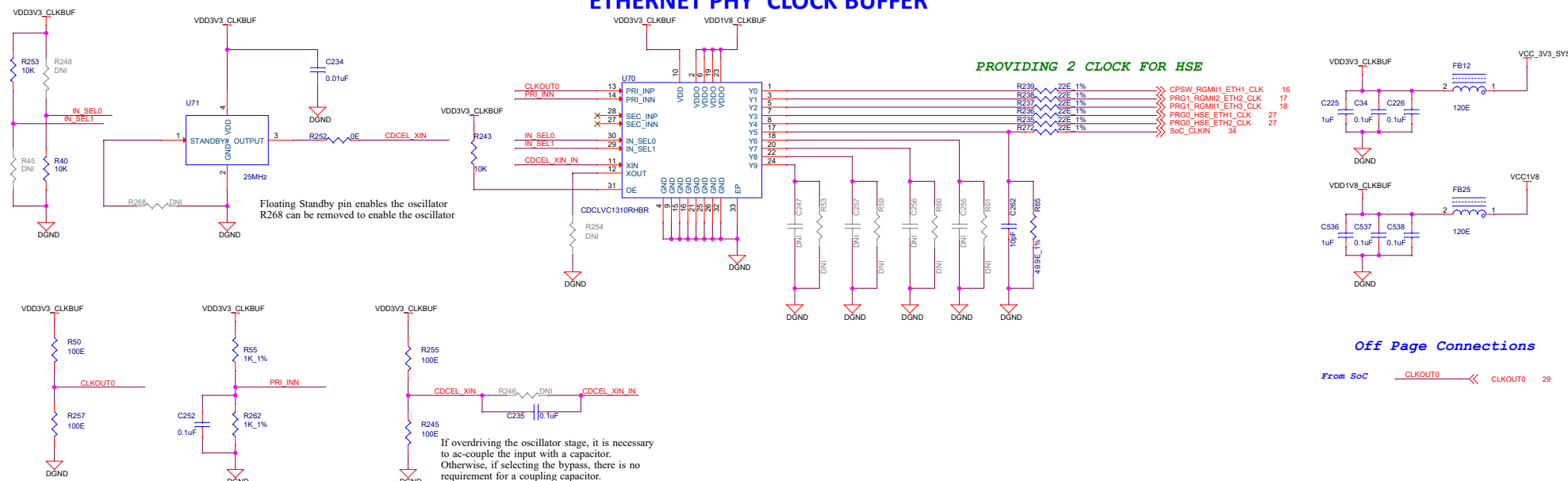
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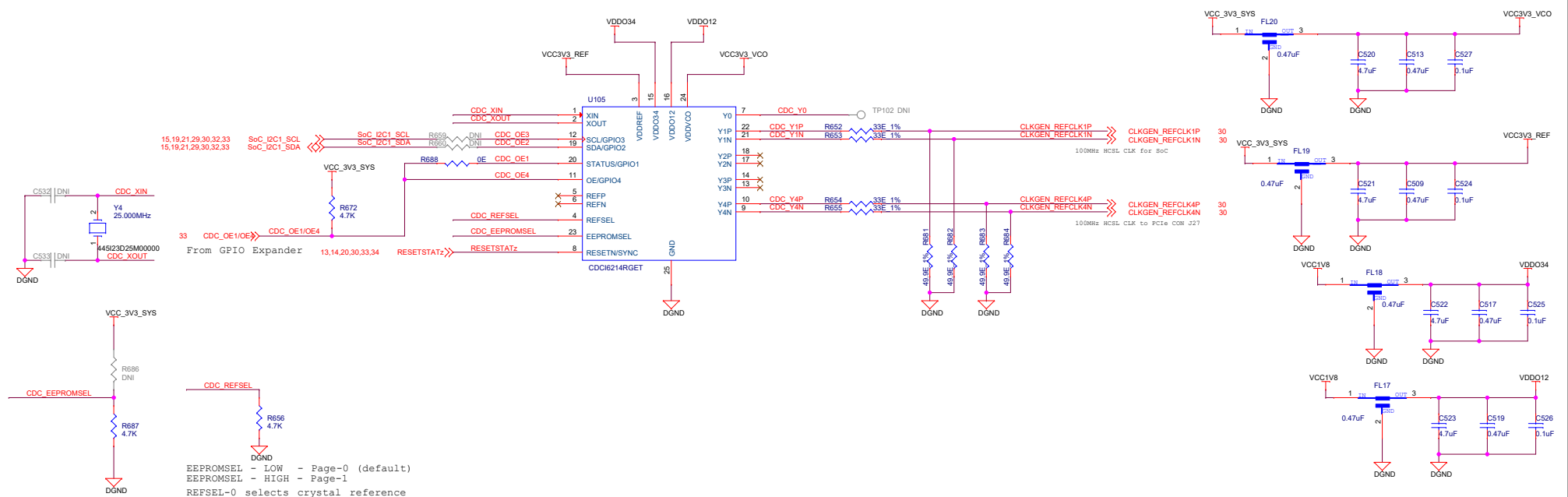
Title		
PCIe INTERFACE		
Size	PROC101C(005) TMS243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 30 of 40

REFERENCE INPUT SELECTION

ETHERNET PHY CLOCK BUFFER



PCIe Clock HCSL (100MHz)



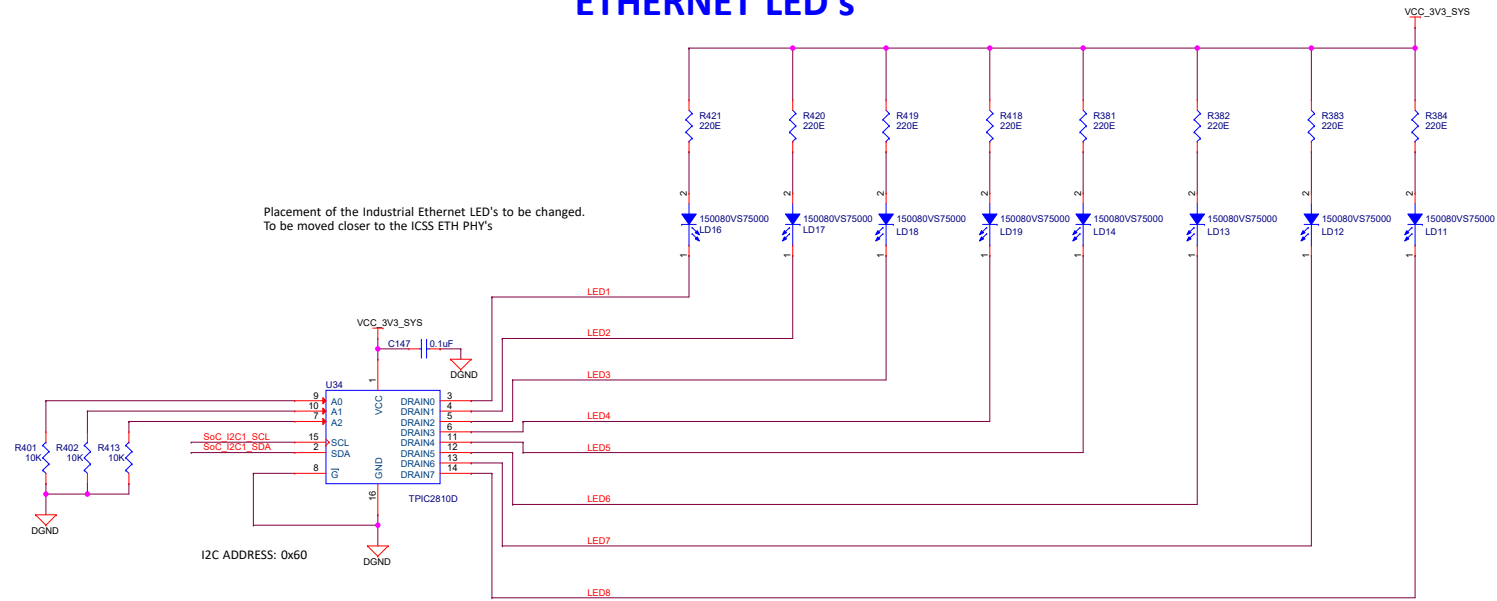
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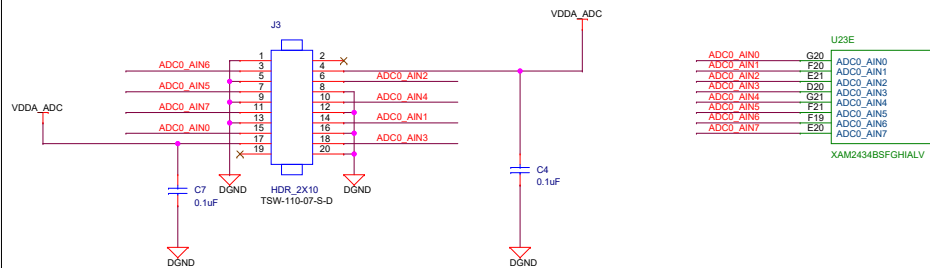
Title ETHERNET PHY & PCIe CLOCK GENERATOR

Size	Variant Name = PROC101C(005) TMD8243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 31 of 40

ETHERNET LED's



ADC CONNECTOR



Off Page Connections

SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,30,31,33
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,30,31,33

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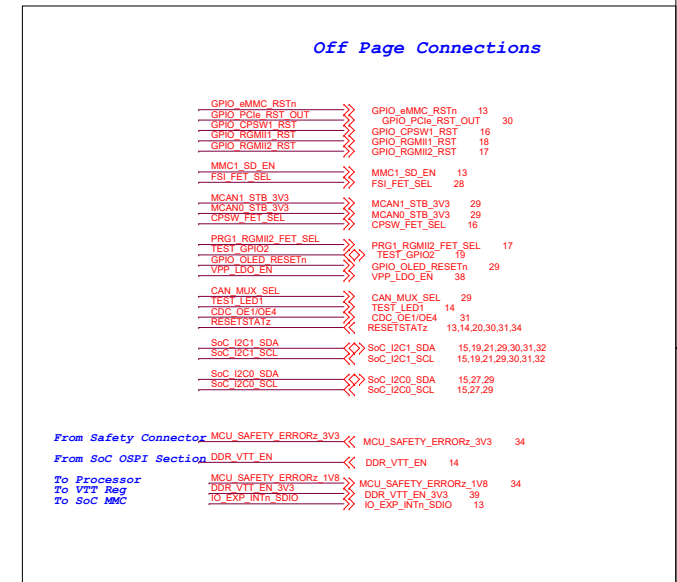
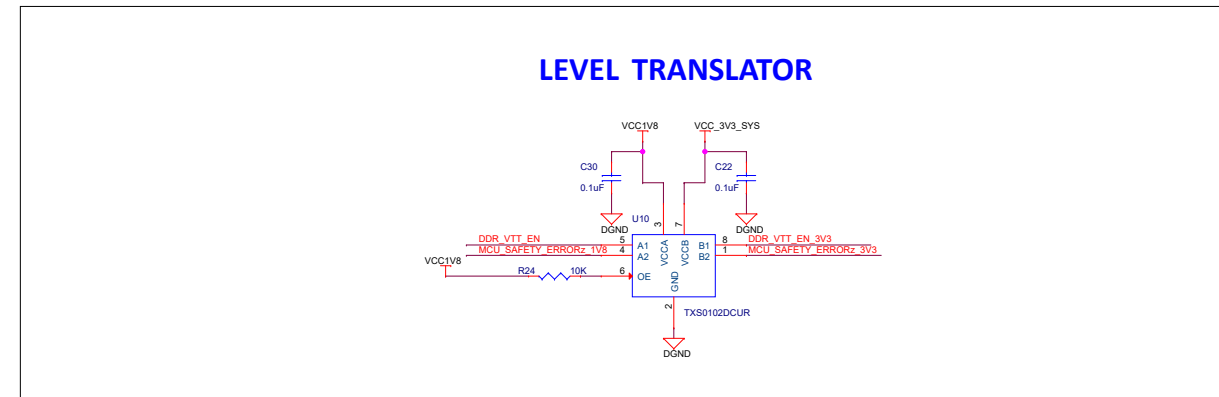
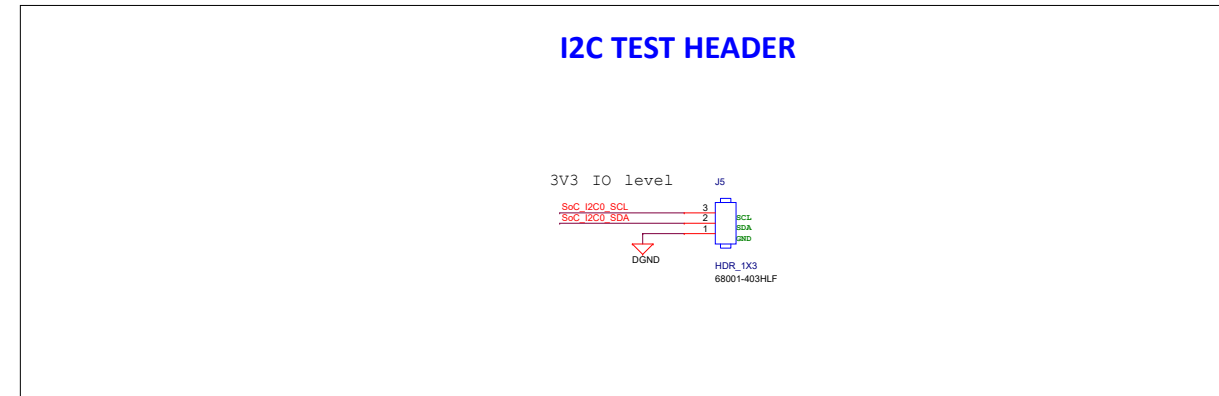
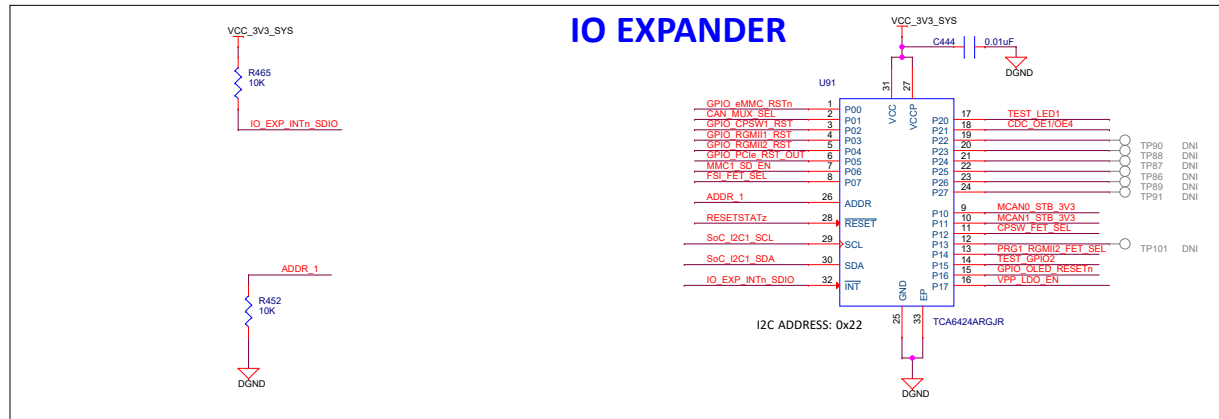
Title: ETHERNET LED's

Size: Variant Name = PROC101C(005) TMD5243EVM

Date: Thursday, August 18, 2022

Sheet 32 of 40

Rev E2



Designed for TI by Mistral Solutions Pvt Ltd



Title IO EXPANDER

Size Variant Name = PROC101C(005) TMD5243EVM

C Date: Thursday, August 18, 2022

Sheet 33 of 40

Rev E2

The schematic shows the MCU_GENERAL section with the following components and connections:

- Resistors:** R309 (4.7K), R311 (4.7K), R303 (4.7K), R306 (4.7K), R593, R594, R597.
- Capacitors:** C487 (10pF), C488 (10pF), C491 (10pF).
- MCU Connections:**
 - I2C0:** MCU_I2C0_SCL, MCU_I2C0_SDA, MCU_I2C0_SCL_RC, MCU_I2C0_SDA_RC.
 - I2C1:** MCU_I2C1_SCL, MCU_I2C1_SDA.
 - SPI0:** MCU_SPI0_CLK, MCU_SPI0_CLK_R, MCU_SPI0_D0, MCU_SPI0_D1, MCU_SPI0_CS0, MCU_SPI0_CS1.
 - GPIOs:** MCU_GPIO0_7, MCU_GPIO0_8, MCU_GPIO0_9, TEST_LED0, MCU_GPIO0_6.
 - UART0:** MCU_UART0_RX_3V3, MCU_UART0_TX_3V3, MCU_UART0_CTS_3V3, MCU_UART0_RTS_3V3.
 - UART1:** MCU_UART1_RX_3V3, MCU_UART1_TX_3V3, MCU_UART1_CTS_3V3, MCU_UART1_RTS_3V3.
- Control Signals:**
 - MCU_RESETz, MCU_RESETSTATz, MCU_RESETReqz.
 - MCU_SAFETY_ERRORz_1V8, MCU_PORz, PORz_OUT, SoC_WARM_RESETz, SoC_WARM_RESETz, RESETSTATz, RESETSTATz.
- Other Components:**
 - U23H, U23C, U35, SN74LVC1G11DCKR.
 - VCC_3V3_SYS, VCC1V8, DGNND, DNI.

The schematic diagram shows the internal wiring of the level translator. On the left, a MOSFET (Q8, IRLML6401) is used to interface the external connection (CONN_MCU_RESETz) with the internal debounce circuit (Debounce_MCU_RESETz). On the right, a push-button switch (SW6, SKHMQLE010) is connected to the MCU_RESETz pin. A 10K resistor (R536) is connected to the MCU_RESETz pin, and a 0.1uF capacitor (C466) is connected to the switch node. The circuit is grounded to DGND.

To HSE Connector	MCU_RESETSTATz	MCU_RESETz	27,35	
		MCU_RESETSTATz	27	
To level translator	MCU_SAFETY_ERRORz_3V3	MCU_SAFETY_ERRORz_3V3		33
To level translator	MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8		33
To Boot Mode Section	PORz_OUT	PORz_OUT	13,16,17,18,20	
From ICSSG Phyl62	PRG1_RGMII_INTn	PRG1_RGMII_INTn	16,17,18	
To User LED	TEST_LED2	TEST_LED2	14	
From Push button	MCU_GPIO0_6	MCU_GPIO0_6	35	
Switch				
	SoC_CLKIN	SoC_CLKIN	31	
	MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	26	
	MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	26	
	MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	26	
	MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	26	

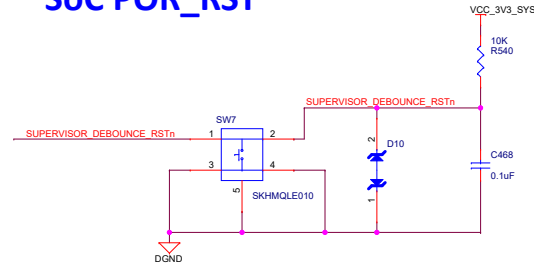
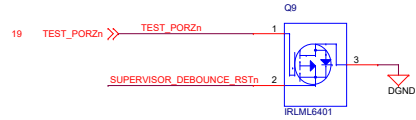


TEXAS
INSTRUMENTS

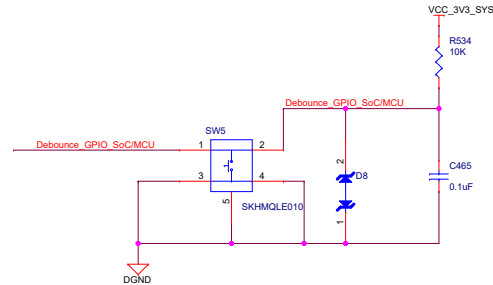
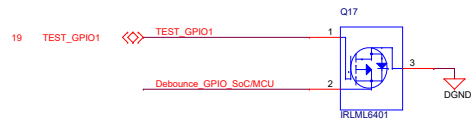
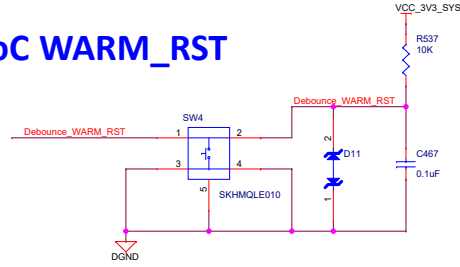
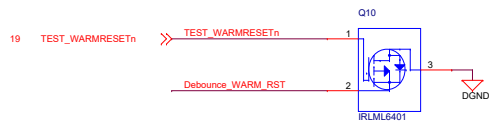


Size	Variant Name = PROC101C(005) TMSD243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 34 of 40

SoC POR_RST

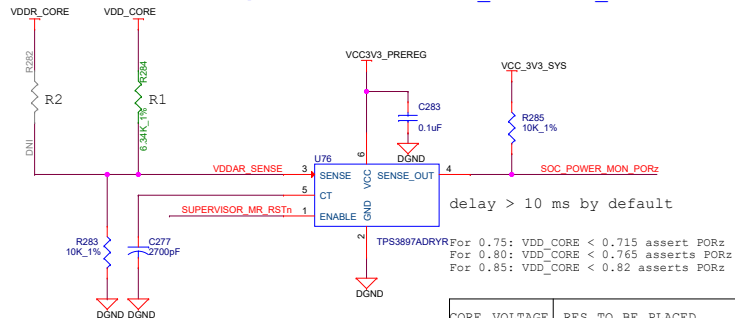


SoC WARM_RST



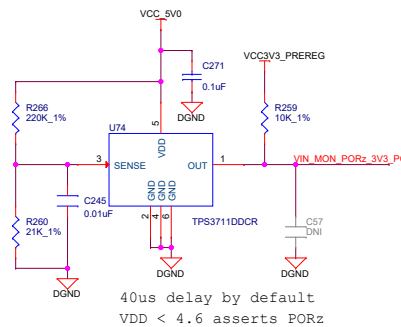
VOLTAGE SUPERVISOR

Core Voltage Monitor (VDDAR_CORE/VDD_CORE)

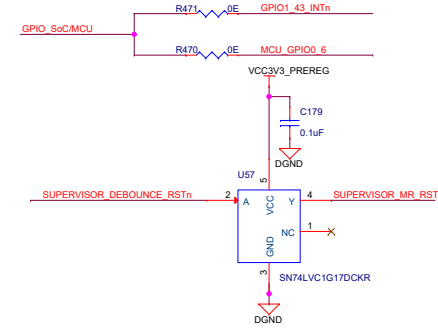
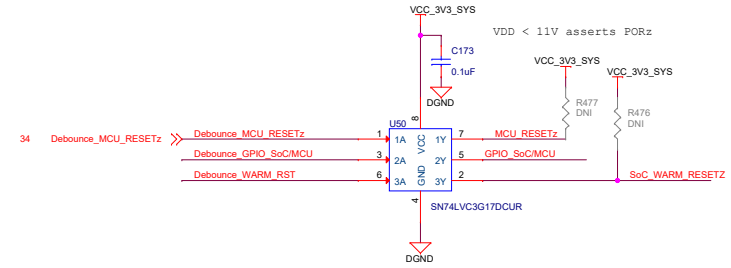


CORE VOLTAGE	RES TO BE PLACED
0.75V	R1 = 4.3K
0.80V	R2 = 5.23K
0.85V	R2 = 6.34K

5V OUTPUT MONITOR (VCC_5V0)

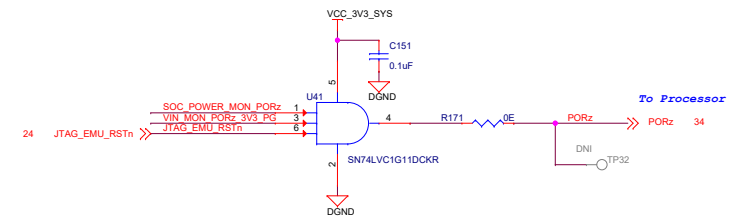


DEBOUNCE CIRCUIT



Off Page Connections

To Processor	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG	37,39
	SoC_WARM_RESETz	SoC_WARM_RESETz	34
	GPIO1_43_INTn	GPIO1_43_INTn	29
	MCU_RESETz	MCU_RESETz	27,34
	MCU_GPIO0_6	MCU_GPIO0_6	34



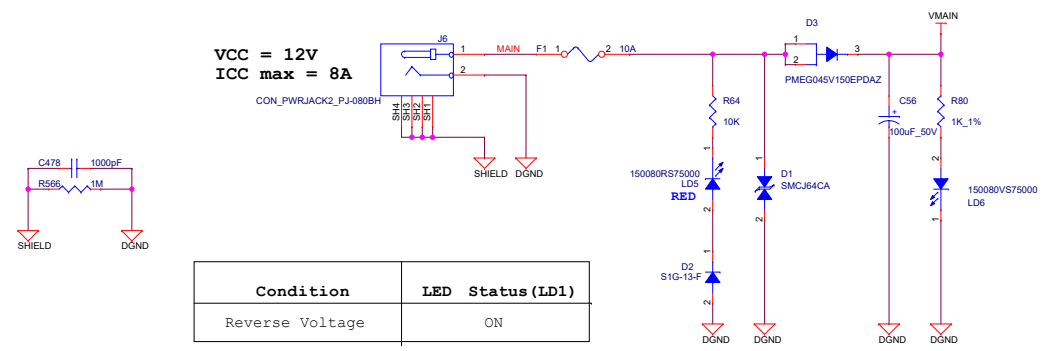
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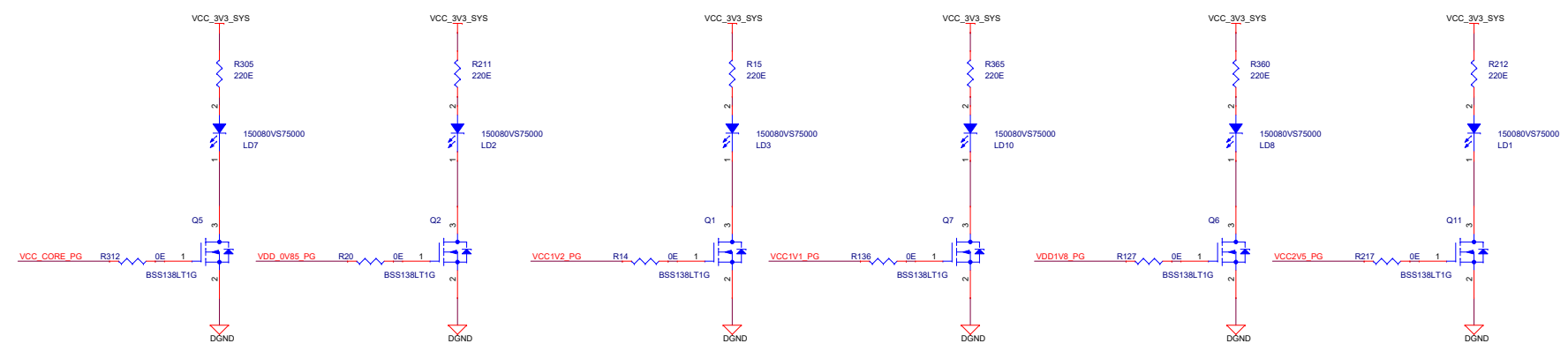
Title DEBOUNCE CIRCUIT & VOLTAGE SUPERVISOR

Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 35 of 40

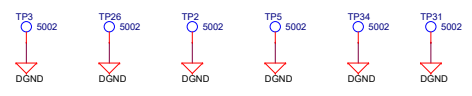
MAIN INPUT 12V DC



POWER INDICATION LED'S



Ground test points



Off Page Connections

VCC_CORE_PG	VCC_CORE_PG	37,38
VDD_0V85_PG	VDD_0V85_PG	38
VCC1V2_PG	VCC1V2_PG	38
VCC1V1_PG	VCC1V1_PG	39
VDD1V8_PG	VDD1V8_PG	38
VCC2V5_PG	VCC2V5_PG	39

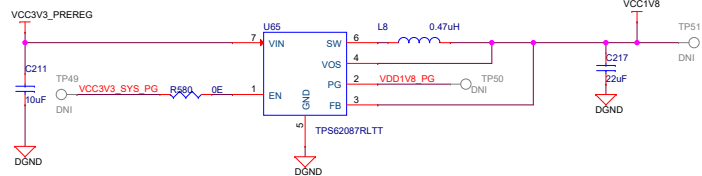
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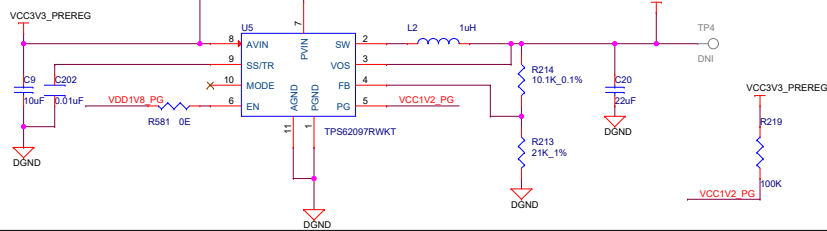
Title MAIN 12V POWERSUPPLY		
Size	Variant Name = PROC101C(005) TMD5243EVM	
C	Rev E2	
Date:	Thursday, August 18, 2022	Sheet 36 of 40

SoC POWER SUPPLY

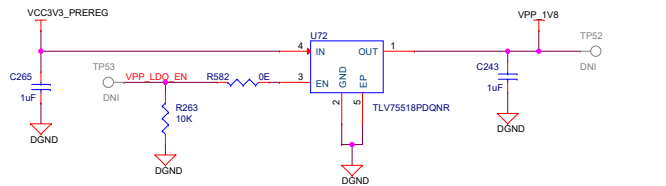
1.8V IO, 3.0AMPS SUPPLY



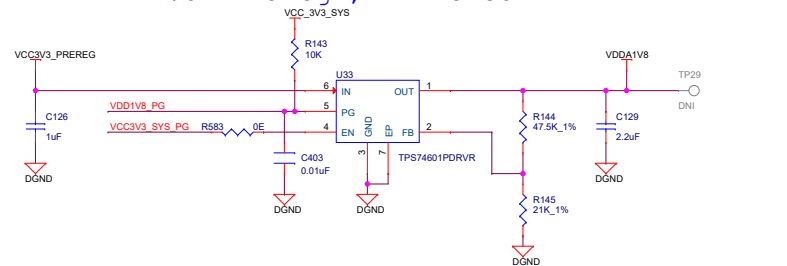
1.2V, 2.0AMPS SUPPLY



1.8V VPP, 0.15AMPS SUPPLY



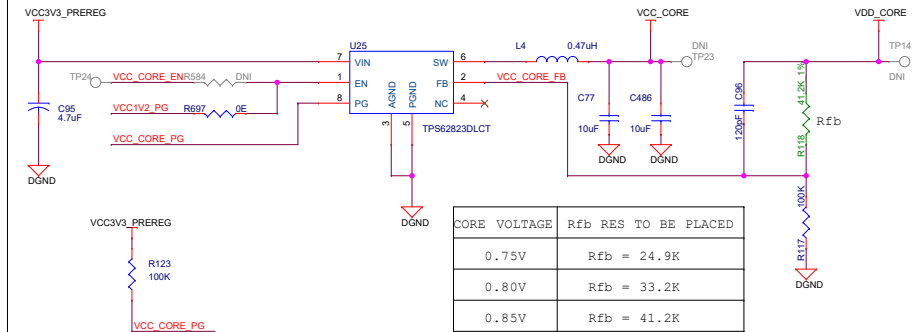
1.8V Analog , 1AMPS SUPPLY



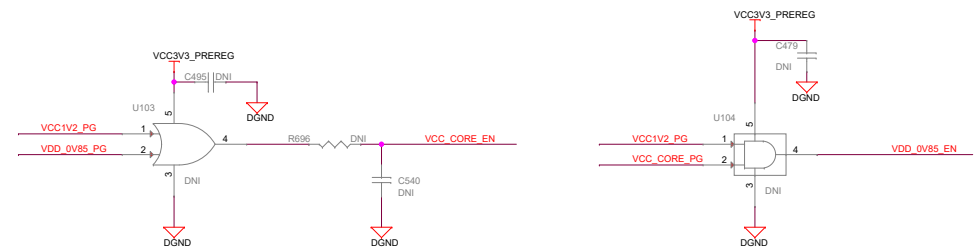
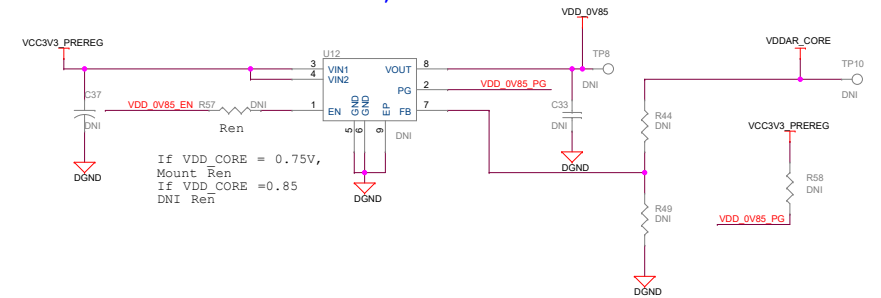
Off Page Connections

36.37	VCC_CORE_PG	VCC_CORE_PG
36	VDD_0V85_PG	VDD_0V85_PG
36	VCC1V2_PG	VCC1V2_PG
36	VDD1V8_PG	VDD1V8_PG
33	VPP_LDO_EN	VPP_LDO_EN
35,37,39	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG
37,39	VCC3V3_SYS_PG	VCC3V3_SYS_PG

0.75 / 0.8 / 0.85V, 3.0AMPS SUPPLY



0.85 V, 1.5AMPS SUPPLY



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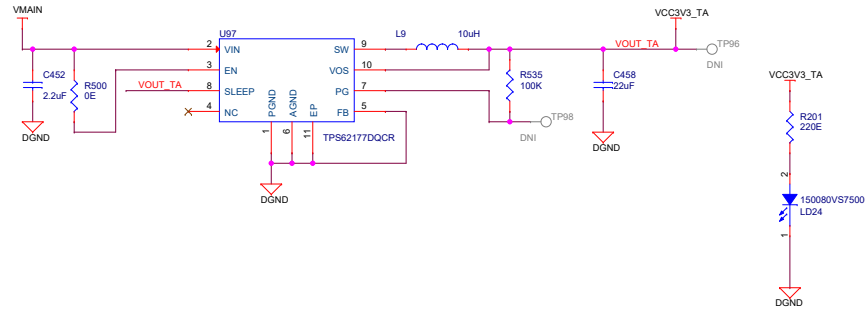


Title SoC POWER SUPPLY

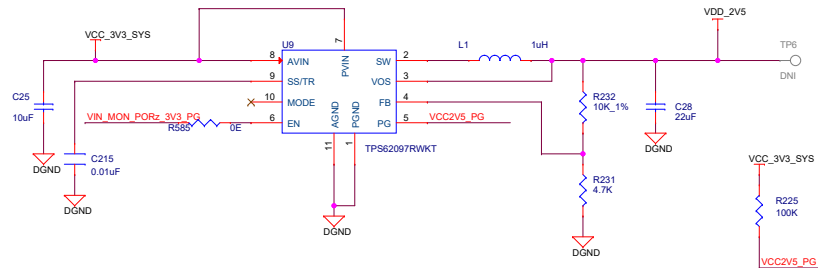
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 38 of 40

PERIPHERAL POWER SUPPLY

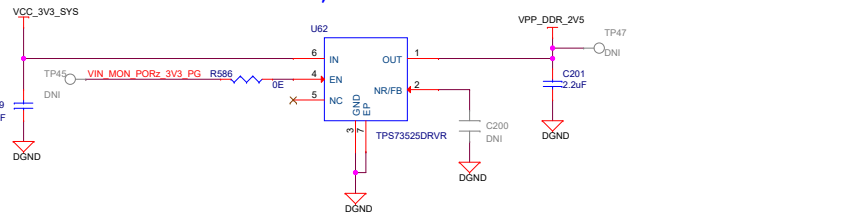
TEST AUTOMATION BOARD POWER



2.5V, 2.0AMPS SUPPLY



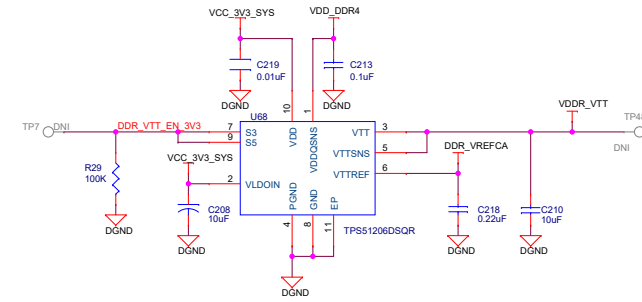
2.5V, .5 AMPS SUPPLY



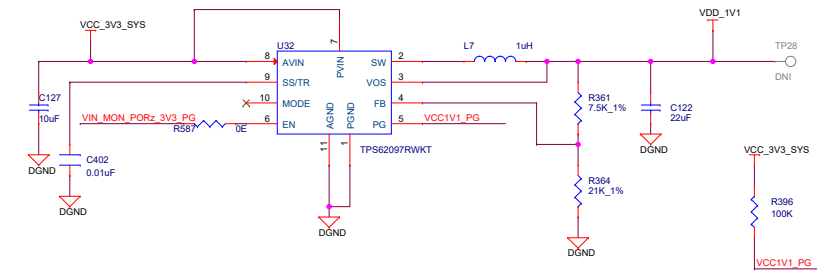
Off Page Connections

33	DDR_VTT_EN_3V3	DDR_VTT_EN_3V3
36	VCC2V5_PG	VCC2V5_PG
36	VCC1V1_PG	VCC1V1_PG
37,38	VCC3V3_SYS_PG	VCC3V3_SYS_PG
35,37	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG

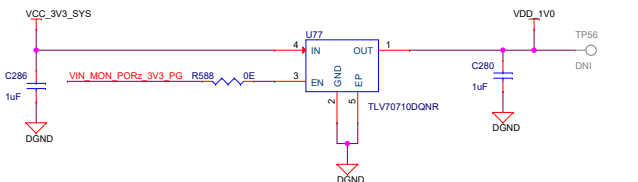
VTT SUPPLY FOR DDR4



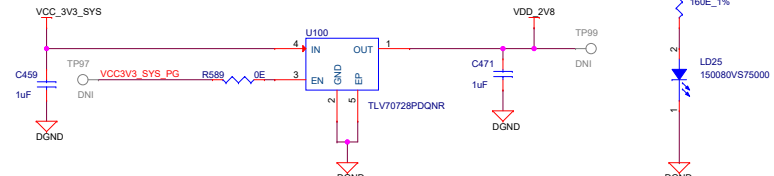
1.1V ETHERNET PHY POWER SUPPLY



1.0V ETHERNET PHY POWER SUPPLY



2.8V , 0.15AMPS SUPPLY



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Title PERIPHERAL POWER SUPPLY

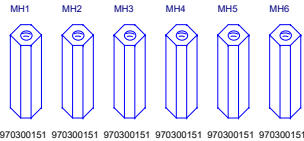
Size	Variant Name = PROC101C(005) TMD5243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 39 of 40

HARDWARE SCHEMATICS

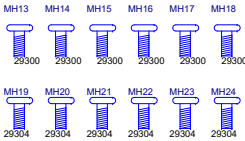
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

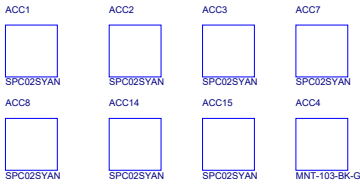
STANDOFFS



SCREWS



JUMPERS



WASHER'S



RUBBER FEET



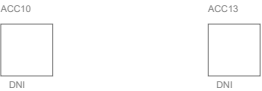
FIDUCIALS



TI EVM FLYERS



Socket & Processor as Accessories



BARE PCB



LABELS

Board Serial No.



Assembly Revision

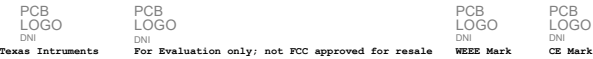


ORDERABLE PART NO



Orderable part number	
Variant	Label Text
001	TMDS64GPEVM
002	TMDS243GPEVM
003	TMDS64HSEVM
004	TMDS64EVM
005	TMDS243EVM

LOGOs



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Title HARDWARE SCHEMATICS

Size	Variant Name = PROC101C(005) TMDS243EVM	Rev
C		E2
Date:	Thursday, August 18, 2022	Sheet 40 of 40